Low Power Glitch Free Delay Lines

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Abstract: The design of the ADPLL must intend to have a phase detection system with higher phase accuracy for minimum phase error. The design should also have easy programmability and calibration along with reduced complexity of the circuit. The paper is based on the basis of being the ADPLL being FPGA realizable. Thus the logic for the ADPLL used should be transferable to FPGA logic and the design of the ADPLL should be hardware implementable. The main aim of the paper is to design and implement ADPLL on FPGA with reducing delay with desired frequency 62.5MHZ.

Keywords— Low power, Glitch, Delay, lines

I. INTRODUCTION

The steady improvement of components for digital signal processing applications, more applications pertaining to processing signals are experiencing a shift from analog to the digital domain. The digital domain compared to the analog domain provide manifold benefits like easy calibration, higher accuracy, better predictability and the probability to increase the complexity without the need for tedious adjustments or calibrations. Thus the digital domain certainly provides a better edge over analog domain which attracts more research and experimentation in this field of study. Due to high integration of very-large-scale integration (VLSI) systems, PLLs often operate in a very noisy environment [1]. The digital switching noise coupled through power supply and substrate induces considerable noise into noise-sensitive analog circuits. Many analog approaches are proposed to improve the jitter performance of PLLs, such as choosing a narrow bandwidth or using a low-gain voltage-controlled oscillator (VCO) [2].

Synthesizers for mobile applications are fractional N-based PLLs. However, those analog approaches often result in long lock-in time and increasing design complexity of the PLLs. The associated fractional spurs must be suppressed, which requires large RC filters and precise loop-gain control when traditional analog techniques are applied. Rapid scaling of CMOS technology enables all-digital PLLs (ADPLLs) implementation. Digital loop filters replace area-consuming RC filters, and the loop gain can be calibrated digitally. However, nonlinear switching and digital transient noise degrade the spur performance.

The frequency synthesizer is a key block used for both up-conversion and down-conversion of radio signals and has been traditionally based on a charge-pump PLL, which is not easily amenable to integration. Recently, a digitally controlled oscillator (DCO), which deliberately avoids any analog tuning voltage controls, was first ever presented in [2] for RF wireless applications. This allows for its loop control circuitry to be implemented in a fully digital manner as first proposed in [2] and then demonstrated as a novel digital-synchronous phase-domain all-digital PLL (ADPLL) in a commercial 0.13µm CMOS single-chip Bluetooth radio.

The phase-locked loop (PLL) has various applications in frequency synthesis, digital modulation, and synchronization, [1], [2]. The PLL can be implemented with analog/mixed signal circuits, or all-digital circuits [1]. The analog/mixed signal PLL can supply high-frequency outputs, but its performance highly depends on the pressure-voltage temperature manufacture conditions. In addition, the phase noise of an analog/mixed-signal PLL may be difficult to control. In contrast to the analog/mixed-signal PLL, the all digital PLL (ADPLL) can be realized with a digital VLSI process, and its performance is easier to control. Moreover, the ADPLL can be easily integrated with a digital circuit system that is useful for many applications such as the baseband communications or electronic equipments.

Recently, all-digital phase-locked loops (ADPLLs) have become more attractive because they yield better testability, programmability, stability, and portability over different processes, and they can reduce the system turnaround time.

II. OVERVIEW OF PLL

The Phase Locked Loop (PLL) is one of the most important building blocks necessary for modern digital communications. It is used as a frequency synthesizer in RF circuits, or to recover time and carrier in the baseband digital signal processing. A thorough understanding of the concept of PLL includes study areas such as RF circuits, digital signal processing, discrete time control systems and communication theory. Phase Locked Loops (PLL) circuits are used for frequency control. They can be configured as frequency multipliers, demodulators, tracking generators or clock recovery circuits. Each of these applications demands different characteristics but they all use the same basic circuit concept.

Phase locked loops were first written about but not implemented in the early 1930’s by a French
engineer named de Bellescize. In 1932 a group of British engineers started developing a receiver based upon de Bellescize’s paper that would be simpler than the super heterodyne receiver that was the best available at the time. Their simple design included a local oscillator, a mixer and an audio amplifier. When the input signal and the local oscillator were mixed at the same phase and frequency the original audio was reproduced from its modulated form. The design was very clever but had its drawbacks. Reception after a period of time became difficult due to frequency drift of the local oscillator. Their solution to this problem incorporated a phase detector comparing the input frequency to the frequency of the local oscillator. The phase detector would output a differential voltage that was fed back into the local oscillator keeping it at the correct frequency. This technique was the same technique that was developed for electronic servo control systems at the time. This was the first iteration in the evolution of the phase locked loop (PLL).

Figure 2.1 contains a block diagram of a basic PLL [11]. It is basically a feedback control system that controls the phase of a voltage controlled oscillator (VCO). The input signal is applied to one input of a phase detector. The other input is connected to the output of a divide by N counter. Normally the frequencies of both signals will be nearly the same. The output of the phase detector is a voltage proportional to the phase difference between the two inputs. This signal is applied to the loop filter. It is the loop filter that determines the dynamic characteristics of the PLL. The filtered signal controls the VCO. Note that the output of the VCO is at a frequency that is N times the input supplied to the frequency reference input.

This output signal is sent back to the phase detector via the divide by N counter. Normally the loop filter is designed to match the characteristics required by the application of the PLL. If the PLL is to acquire and track a signal the bandwidth of the loop filter will be greater than if it expects a fixed input frequency. The frequency range which the PLL will accept and lock on is called the capture range. Once the PLL is locked and tracking a signal the range of frequencies that the PLL will follow is called the tracking range. Generally the tracking range is larger than the capture range. The loop filter also determines how fast the signal frequency can change and still maintain lock. This is the maximum slewing rate. The narrower the loop filters bandwidth the smaller the achievable phase error. This comes at the expense of slower response and reduced capture range.

### III. GLITCH FREE DELAY LINES

The basic aim of this paper is to avoid glitches present in the circuit which is constructed using universal gate. Power is also analysed to maintain low power consumption. Many methods are used to remove glitches present in the circuit. Delay has been reduced by using delay cell in each element of circuit and power consumption also reduced by microwind technology. Presence of glitch may cause unwanted transition in the circuit result. Jitter also because undesirable deviation of periodic signal it may also results glitches in the circuit. Jitter may be caused by interference of the signal and crosstalk with carriers of other signals.

Digital to analog converters or analog to digital converters used and time between samples varies. Time resolution of digital signal is higher than the voltage resolution of analog signal. Digitally controlled delay technique plays a role in analog to digital converters in circuit. In each element of circuit delay cell is constructed to reduce the output delay. A delay element is discrete element which allows signal to be delayed number of samples. Power consumption of both NAND and NOR circuit is analyzed and it is less existing NAND based circuit. Minimizing the delay of circuit depends on the number of delay. Output capacitance and drivability of delay elements are the key parameters for designing low jitter delay elements. Each circuit can be constructed using NAND and NOR gate maintain same resolution with minimum delay produced. Delay element constructed using regular cascade of cells. It has simple layout organization with low nonlinearity effects. Hence removal of glitch in circuit and low power consumption of universal circuit has proposed. A portable Digitally Controlled Oscillator Using Novel Varactor.

A portable digitally controlled oscillator by two input NOR gate as a digitally controlled varactor in fine tuning delay cell design. It uses gate capacitance under different digital control inputs with delay resolution 256 times better than single resolution time. Phase locked loop used in many communication systems to clock and data recovery or frequency synthesis. To process high resolution digitally controlled oscillator by using NAND /NOR gate as novel varactor. Resolution is non-uniform and sensitive to power supply variation. It has high portability and short design turnaround cycle and also has small size of varactor. The driving strength can be changed by using capacitance loading. Low Cost Variable Delay Line for Impulse Radio Ultra Wide Band Architecture introduces delay line circuit suitable for impulse radio ultra wideband architecture. Fine synchronization used to be related to relative high cost devices. Low power architecture has been tested by commercial off the shelf breadboard. This achieves good performance and delay step in nanosecond range. Its band width is greater than
0.25MHz which is more than radiated spectrum. Additional circuit is needed to perform full clock cycle. Reference voltage can be adjusted with digital to analog converter. High data rate and low power system of wireless networking developed by using local area networking. This technique is based on broadcasting of very low power signals. Simple hardware is added to reduce latency. Delay is up to 40% of pulse width. Incoming signal delay depends on threshold voltage. Design is simple and fast circuit implementation.

All Digital Phase Locked Loop for High Speed Clock Generator. It uses both a digital control mechanism and ring oscillator can be implemented with standard cells. Power dissipation is about 100mW with 3.3 power supply. Phase locked loop is widely used for frequency synthesis application. Jitter is less than ±4% of clock cycle and also it avoid functional failure of the system. Adaptive algorithm can be used to achieve fast lock in time. It yield better testability, programmability, stability and portability over difficult process and reduces turnaround time. Loop filter detects the maximum and minimum control code. Resolution improved about 5 ps by adding fine tuning delay cell. It has fine tuning range. Controllable range of fine tuning delay cell should cover coarse tuning. Control code has small variation due to input jitter. Fast locking achieves 41 refresh cycles has better portability. It is suitable for on chip application. Pulse amplifier effectively minimize dead zone of the signal.

**Removal of Glitch in circuit**

Glitching problem will occur when the control code of circuit struck at some values and it gives error values at the output. Glitching problem can be solved by raising the control values of the cells in each element of the circuit.

\[
\delta = 2t_{\text{tand}} + 2t_{\text{tand}} + c
\]

Where \( t_{\text{tand}} = \frac{t_{\text{tand LH}} + t_{\text{tand HL}}}{2} \)

While \( t_{\text{tand LH}} \) and \( t_{\text{tand HL}} \) represent the delay of each NAND gate for low to high and high to low output commutation respectively. When delay cell is passed to output of third element of gate it becomes post turn state and all other state become turn state. Signal propagates from input to output of the circuit through gates. Dummy cells are used to maintain load balancing in the circuit. The NAND gate is used to reduce the hardware of circuit. Any gate can be constructed with help of NAND gate. It is very useful for construction of digital circuits.

**Fig.3.1 Inverting Glitch Free Circuit of NAND Gate**

The circuit eliminates the presence of glitches by using dummy cells in each element of circuit. Control bits can in one of the three possible states. In pass state the circuit with universal gate of third element gives output 1 and fourth element makes the signal propagate to low level of gates in the circuit. In this figure all the NAND gates present same load and gives same delay. Delay is given by

**Fig.3.2 Non Inverting Glitch Free Circuit of NAND Gate**

In many applications output glitching can be avoided by synchronizing both input and output values. Minimizing the arrival time of control bit values than input values to reduce the delay time of each element

**IV. RESULTS**

Conventional DCDL

**Fig.4.1: Block diagram of the conventional DCDL with one control**

In the figure 4.1 the cell which is denoted by —A‖ is the fast input of the NAND gate. Gates denoted by D‖ is the dummy cell for the load balancing. These delay elements are controlled by one bit control code c to propagate the delay. When the delay control code C increased by 1, multiple propagation path within the DCDL structure generates leads to more glitching in the delay line. The control bit \( S_i = 0 \) (pass state), \( S_i = 1 \) (turn state). In DCDL applications, to avoid DCDL
output glitching, the switching of delay control-bits is synchronized with the switching of the input signal. Glitching is avoided if the control bits arrival time is lower than the arrival time of the input signal of the first DE which switches from or to the turn-state.

The above fig 4.2 The DEs i=c with are in pass-state (Si =0,Ti =1). In this state the NAND 3|| output is equal to 1 and the NAND 4|| allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state (Si=Ti=0). In this state the upper input of the DE is passed to the output of NAND 3||. The next DE(i=C+1) is in post-turn-state. In this DE the output of the NAND 4|| is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND 3|| through NAND 4||. All remaining DEs (for i>C+1) are again in turn-state. The simulation results shows that the proposed NAND based DCDL confirms the glitch free propagation in the delay elements.

In above fig 4.3 non inverting DCDL as many applications output glitching can be avoided by synchronizing both input and output values. Minimizing the arrival time of control bit values than input values to reduce the delay time of each element.

In this circuit the NAND gates “1” and “2” of the first DE have been deleted, together with signal. The signal of the second DE is now equal to in therefore the whole behaviour of the DCDL is non-inverting

V. CONCLUSION

The glitch free DCDL is implemented in the ADDLL circuit. Glitches in the delay units are avoided by the above discussed timing constraints of the control code. Arrival of the input control code is
designed as that the propagation of the signal through the gates does not produce glitches. Driving circuits for the control codes are also designed that the difference in the driving control bits are designed with the proper timing constraint and delay. The implemented ADDDLL is registering based DLL. The glitch free DCDL is implemented in the ADDDLL circuit. Glitches in the delay units are avoided by the above discussed timing constraints of the control code. Arrival of the input control code is designed as that the propagation of the signal through the gates does not produce glitches. Driving circuits for the control codes are also designed that the difference in the driving control bits are designed with the proper timing constraint and delay. Thus with this the NAND based delay line is implemented with glitches and without glitches for the comparison of the output. Thus with this the glitches can be well studied and analysed for the better delay circuits.

References


Author’s Profile

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