Comparative Analysis of PLL for RF Applications

Pallavi Patil#1, Virendra K. Verma #2,
# M.tech Scholar, Asst. Professor, Electronic & Communication Department
Sanghvi Institute of Management & Science, Indore (India)

Abstract— Among the many different frequency synthesis techniques, the dominant method used in the wireless communications industry is the digital PLL circuit. Compared to the analog techniques used in the infancy of frequency synthesis, the modern PLL is now a mostly digital circuit. Phase Locked Loop (PLL) is a fundamental part of radio, wireless and telecommunication technology. The goal of this document is to review the theory, design and analysis of different DPLL circuits. The digital phase locked loop, DPLL, is a circuit that is used frequently in modern integrated circuit design. This paper presents optimized comparison of different Digital Phase Locked Loops (DPLL) for generating RF carrier signal used for phase demodulation.

Keywords— Phase locked loop, digital phase locked loop, flip-flop DPLL, Nyquist-rate DPLL, Lead-Lag DPLL, Exclusive-OR DPLL, Zero-crossing DPLL.

I. INTRODUCTION

Phase locked loop is a technique which has contributed significantly toward the technology advancement in communication and motor servo control system in the past 30 years. Inventions in the PLL schemes combining with novel integrated circuit (IC) technology have made PLL devices important system components.

Basic PLL

A PLL is a device which causes a signal to track another one. It keeps an output signal synchronizing with a reference input signal in frequency as well as in phase. More precisely, the PLL is simply a servo system, which controls the phase of its output signal in such a way that the phase error between output phase and reference phase reduces to a minimum. [7]

PLL Components

The four basic components of a PLL circuit are the VCO, the phase-frequency detector, the main and reference dividers, and the loop filter. This is called 1st order PLL or Type 1 PLL. It suffers from limited acquisition range. So to eliminate this problem, Phase frequency detector along with charge pump is replaced by phase detector.

Fig (1) Block diagram of Phase Locked Loop

Functionality of all these blocks is explained below:

A. Phase Frequency Detector (PFD)

The purpose of phase frequency detector is to detect the phase and frequency between input signal and feedback signal and generates error which is equal to phase deviation between them.

B. Charge Pump

Charge pump is a kind of DC convertor that uses capacitor as energy storage element. Signals coming from PFD are applied to charge pump to steer the current into and out of capacitor causing voltage to increase or decrease accordingly.

C. Loop filter

Output voltage from passive filter is control voltage of VCO which increase/decrease frequency in such a manner that voltage output is maintained proportional to charge of the capacitor [2].

D. Voltage Controlled Oscillator (VCO)

This is the most important block of PLL system that helps to produce output frequency according to voltage. VCO is fully differential based ring oscillator consisting of three parts i.e. voltage to current convertor, current controlled oscillator (CCO) and level shifter.

E. Loop Divider

This block provides greater flexibility to design engineers by operating PLL system at higher frequencies. Also it is used to reduce frequency coming from VCO.

II. CLASSIFICATION OF DPLL

The DPLLs can be also classified according to the mechanization of the phase detector into five types as follows [8]

1. The flip-flop DPLL (FF-DPLL):

In this type the phase detector is realized by a set-clear flip-flop and counter.

Fig (2) Block diagram of the flip flop DPLL

2. The Nyquist-rate DPLL (NR-DPLL):

In this DPLL the sinusoidal input signal is sampled uniformly at the Nyquist rate fs and converted to N-bit
digital signal by an analog-to-digital converter (ADC), and then it is multiplied digitally by the DCO output \( v(k) \) to form an error signal. This error signal is applied to N-bit digital filter whose output controls the period of the DCO.

Fig (3) Block diagram of the Nyquist-rate DPLL

3. The lead-lag DPLL (LL-DPLL), a.k.a binary-quantized DPLL (BQ-DPLL):
The LL-DPLL is characterized by the binary output of the phase detector that indicates whether the DCO waveform leads or lags the input signal. Due to this quantization it is often named “binary quantized DPLL”. The input sinusoidal signal should be converted to a square wave by a comparator. On the occurrence of a DCO pulse, either “lead” or “lag” terminal of the phase detector will give a pulse depending on the state of the input signal being “high” or “low”, respectively. These pulses are applied to a special type of digital filters known as “sequential filter.” The sequential filter deals with the input “lead” and “lag” pulses statistically; it observes them for a variable duration of time and gives a decision when a reliable limit is reached.

Fig (4) Block diagram of the lead-lag DPLL

4. Exclusive-OR DPLL (XOR-DPLL):
Greer has utilized an exclusive-OR gate as a phase detector. He used a K-counter as a digital filter and an increment-decrement (I/D) counter with a divide-by-N counter as a DCO.

Fig (5) Block diagram of the Exclusive-OR DPLL

5. Zero-crossing DPLL (ZC-DPLL):
This type of DPLLs accepts sinusoidal signals and samples the input signal at or near zero crossings, hence the name zero-crossing DPLL (ZC-DPLL). There are two variations of ZC-DPLLS. The first, named ZC1–DPLL, samples only on the positive-going zero crossings, while the other type, ZC2–DPLL, samples on both positive and negative-going zero crossings.

Fig (6) Block diagram of Zero-crossing DPLL (ZC1-DPLL)

### III. TABLE (1)
Comparative analysis of different types of DPLLS

<table>
<thead>
<tr>
<th>DPLLs (PARAMETER S)</th>
<th>Flip-flop DPLL/FFD PLL</th>
<th>Nyquist-rate DPLL (NR-DPLL)</th>
<th>Lead-lag DPLL (LL-DPLL)</th>
<th>Exclusive OR DPLL (XOR-DPLL)</th>
<th>Zero-crossing DPLL (ZC-DPLL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLOCKS USED</td>
<td>Phase detector, loop filter, digital control</td>
<td>ADC, loop filter, algorithmic DCO</td>
<td>Phase detector, loop filter, divide counter</td>
<td>Phase detector, filter, divide counter</td>
<td>ADC, loop filter DCO</td>
</tr>
<tr>
<td>PHASE DETECTOR (PD) USED</td>
<td>Flip-flop counter type</td>
<td>Analog to digital converter</td>
<td>Phase frequency detector</td>
<td>Exclusive OR gate type</td>
<td>Phase detector</td>
</tr>
<tr>
<td>LOOP FILTER</td>
<td>Digital filter</td>
<td>N-bit digital filter</td>
<td>Sequenntial filter</td>
<td>K counter</td>
<td>N-bit digital filter</td>
</tr>
<tr>
<td>ADVANTAGE</td>
<td>N-bit outputs are possible.</td>
<td>It has simple structure.</td>
<td>It is easily adapted to operate in conjuncti on with an XOR phase detector.</td>
<td>It perfectly works as an integrator.</td>
<td>Good control over hold range and lock in range.</td>
</tr>
<tr>
<td>BAD VANTAGE</td>
<td>Circuit is not simple. It requires three frequency inputs.</td>
<td>It does not offer jitter design criterion.</td>
<td>It does not perfectly work as an integrator.</td>
<td>It does not operate with other detectors except XOR or JK FF.</td>
<td>It is not suitabl e for software implementatio ns.</td>
</tr>
</tbody>
</table>
Apart from the classification of different DPLLs there are various other circuits of DPLL which are different from one another in different sections. I have given my best to put a brief comparative analysis among the different DPLLs circuits described in the papers.

IV. TABLE (2)
Performance comparison of different DPLLs used in various papers

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TECHNOLOGY</td>
<td>0.45um</td>
<td>0.25 um</td>
<td>0.35 um</td>
<td>IP3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CM</td>
<td>OS</td>
</tr>
<tr>
<td>POWER DISSIPATION</td>
<td>@210MHz</td>
<td>@500MHz</td>
<td>25 mW</td>
<td>900 (uW/ MHz)</td>
</tr>
<tr>
<td>SUPPLY VOLTAGE</td>
<td>1.2V</td>
<td>3.3V</td>
<td>1.9V</td>
<td>3.3V</td>
</tr>
<tr>
<td>FREQUENCY</td>
<td>6.54-105MHz</td>
<td>45-510MHz</td>
<td>8.5-660MHz</td>
<td>300 MHz</td>
</tr>
</tbody>
</table>

V. APPLICATIONS of PLLS

Phase-locked loops are widely used for synchronization purposes:

- In space communications for coherent demodulation and threshold extension.
- Phase locked loop can also be used to demodulate the frequency modulated signals.
- In radio transmitters, a PLL is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency.
- Demodulation of AM and FM signals.
- Recovery of small signals that otherwise would be lost in noise (lock in amplifiers to track the reference frequency)
- Recovery of clock timing information from a data stream such as from disk drives.
- Clockmultipliers in microprocessors that allow internal processor elements to run faster than

external connections, while maintaining precise timing relationships.

VI. ADVANTAGES OF DIGITAL PHASE LOCKED LOOP

Digital PLLs (DPLLs) are attracting more attention for the significant advantages of digital systems over their analog counterparts. These advantages include superiority in performance; speed, reliability, and reduction in size and cost. DPLLs do not suffer from the sensitivity of the voltage-controlled oscillator (which decides the center frequency) to temperature and power supply variations, hence the need for initial calibration and periodic adjustment. DPLLs can operate at very low frequencies that create problems in APLLs.

VII. CONCLUSION

This paper serves as an introduction for this DPLL special section. It provides a concise review of the basic DPLL principles applicable to communication and servo control system gives the configuration of DPLL applications and reports a number of popular DPLL chips. This paper has only talked about the comparison of different digital phase locked loop circuits. The implementation of these circuits will be done in the future work. There are many improvements and concepts that still need to be learned, but the basics of all DPLLs implementation are covered during this project.

ACKNOWLEDGEMENT

I have taken efforts to make this study. As with any enterprise, this research work could not have been completed without help and support of others. I would like to thanks my research advisor Mr. Virendra Verma for his valuable contributions.

REFERENCES

[4] A 300MHz Direct Digital Frequency Synthesizer Based on Improved Redundant prediction CORDIC in 0.35um CMOS Pei-Lin Liu1*, Yi-Ding Huang2, Yue Huang3, Shu-Qin Wua,78-1-4244-5798-4/10/$26.00 ©2010 IEEE
[5] Design of a PLL Based Frequency Synthesizer for WiMAX Applications Mohsen Tamaddon, Milad Ataei,


