Design Analysis of 1-bit Comparator using 45nm Technology

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Abstract: This paper presents the design and analysis of an efficient 1-bit comparator. The design of comparator uses XNOR gate which is static energy recovery and AND gate based on pass transistor logic (PTL). The proposed comparator comprises of 3 PMOS and 7 NMOS transistors. The total chip area covered by the proposed comparator is less as compared to the conventional design. The comparator has been designed in logic editor and it is simulated utilizing 45 nm fabrication technology. Simulation of Schematic design and the parametric investigation has been done after the initial testing of the design. Two design methodologies are employed while designing the comparator i.e. fully automatic layout & Semi custom layout design techniques. Analysis of these different designs is done on some of the basic performance parameters, which are compared in terms of power consumed, delay and number of transistors used. In this paper a technique for design and analysis of comparator is presented and result reflects that it serves good quality of design in comparison of conventional MOS approach. So it gives less power consumption as around 63% and delay of around 50.6% less than that of conventional MOS device.

Keywords: Magnitude Comparator, Digital Comparator, CMOS, Power Dissipation, Pass Transistor Logic, Digital Integrated Circuits, VLSI design.

1. INTRODUCTION

COMPARATOR in digital systems is very common and needful arithmetic component to compare the input signals. There are various ways by which we can design CMOS comparators, which is having different area utilization, operating speed, power consumption, and circuit complexity. Individual can design the comparing circuit by optimizing the logical function which can be applicable for short inputs comparator circuit only and by using this approach for the larger input comparator circuit; there is an abrupt increase in circuit complexity which in turn degrades the operating speed to a great extent [1]. A digital comparator is an electronic device, which gives the output equivalent values depending on the applying two bits as input signal and performs applicable test on those signals to determine their comparison to each other. As we lives in the technological world, where we need the advanced technology to fulfill our requirement. So demands of these newest technologies and the advanced convenient devices increases day by day very rapidly. As we talk about the VLSI technology, in this environment the device should be fabricated in such a way that it should be of higher speed, less in cost, very small chip size, low power consumption and reliable in all aspects. Many of the electronic devices like mobile devices and other portable computing devices have constraints in terms of Power and area consumption. To overcome the constraints, several logic styles have been developed to improve area and power consumption. The performance estimation of comparator is based on the design criteria for specific application. The main issues in performance estimation are area consumption, propagation delay, power dissipation and power delay product. In CMOS comparator design there are some points of consideration like chip size, speed, power consumption are taken into account. In VLSI development cycle, main issues are power consumption & heat dissipation. To avoid these problems it is necessary to lower down the voltage level of power supply, switching frequency and transistor capacitance [2]. A Pass Transistor Logic (PTL)-based circuit which utilizes only one kind of transistor i.e. NMOS, is Complementary pass-transistor logic (CPL). This style of using CPL gives great functionality which can reduce the no. of transistor count in the circuit [3]. It is very important that a designer have to choose very basic and simple logical arithmetic solution to optimize the chip circuit [4]. CPL comprises of complementary I/O, a NMOS PTL network, & CMOS output inverters [5]. These performance criteria should be individually investigated, analyzed for the various design of the comparator by different logic style. Power dissipation in any comparator is due to two components, one is static dissipation which occurs due to leakage current, second is dynamic dissipation that occurs because of switching transient current & charging and discharging of load capacitance. In CMOS circuits, power dissipation is mainly due to dynamic power dissipation.
dissipation. We have the formula for calculate the average dissipated dynamic power \( P_d \), which is proportional to energy required to charge and discharged the circuit capacitance \( C_L V^2_{\text{DD}} \) and inversely proportional to the switching time \( t_p \).

\[
P_d = C_L V^2_{\text{DD}} / t_p
\]  

(1)

From solving above equation we also find the total power dissipation which is another equation and is given as the sum of static and dynamic powers plus short circuit dissipation.

\[
P_T = P_s + P_d + P_{scd}
\]  

(2)

The average propagation delay of the inverter is given by \( \tau_p \) which is defined as the average time required for this input signal to propagate through the inverter.

\[
\tau_p = (\tau_{\text{PHL}} + \tau_{\text{PLH}}) / 2
\]  

(3)

From above equation we observed that:

\[\tau_{\text{PHL}} = \text{Input to output signal propagation delay during the high to low transition}\]

\[\tau_{\text{PLH}} = \text{Input to output signal propagation delay during the low to high transition}\]

And from that, the power delay product is also defined as

\[
PDP = 2 P_{\text{avg}} * \tau_p
\]  

(4)

II. CMOS COMPARATOR

Digital comparator also called magnitude comparator is a combinational circuit that compares two input binary bits (A and B) and generates the outputs to indicate whether both the inputs are equal, A is smaller than B and A is greater than B [6]. So the circuit has three outputs to indicate whether \( \text{A=B} \), \( \text{A<B} \) and \( \text{A>B} \). So we have the three different outputs equal to logic high according to any given input sequence [7].

<table>
<thead>
<tr>
<th>input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

From the truth table it can be observed that:

\[
E = \text{A XNOR B}
\]  

(5)

\[
G = \overline{\text{AB}}
\]  

(6)

\[
L = \overline{\text{A}}\overline{\text{B}}
\]  

(7)

And the implementation of the above function using Logic gate is shown below as:

In figure above, if we give \( 2^n \) input at the input of comparator, then total possible states are \( 2^{2n} \). In which 2\(^{n}\) equal state \( \text{A=B} \) and \( (2^{2n}-2^n)/2 \) is \( \text{A<B} \) or \( \text{A>B} \) state. Here we are using 1-bit comparator circuit for analysis, so the truth table based on that is given below as:

![Fig. 2 Logic diagram of 1-bit comparator](http://www.ijettjournal.org)

Figure 2 shows the Logic diagram of 1-bit comparator. As the theory suggests that conventional CMOS circuit technology consists of two type of transistors (devices) one is NMOS transistor and another is PMOS transistor. Transistor operation is based on electric filed so the devices are called Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Two important characteristic of CMOS are high noise immunity and low static power consumption [8]. According to the research, the complementary gate CMOS circuit has an NMOS pull-down network which connects the output to 0 (GND) and also has a PMOS pull-up network which connects to output 1(VDD). A simple structure of pull-up and pull down network is shown below in figure 3 as:
III. COMPARATOR SCHEMATIC

1 bit comparator using conventional MOS logic is designed on Cadence shown in fig 4 and 5 respectively, in which In1 and In2 is used as inputs and three Out1, Out2, Out3 as output. In whole circuit 8 MOS device (4 PMOS and 4 NMOS) for XNOR which gives equal state output, here two inverter for A and B which used as input of XNOR. For A<B here have used 4 MOS devices (2 NMOS and 2 PMOS) and similarly for A>B 4 MOS device (2 NMOS and 2 PMOS) are used as shown in figure below:

![Fig. 3 General logic gate using pull up and pull down networks](image)

![Fig. 4 Schematic of 1-Bit comparator using conventional CMOS logic](image)

In this paper two different schematic design using CMOS logic and PTL logic is created. In complex VLSI design manual designing for a very complex circuit will become very difficult. So as compared to manual layout designing an automatic design generation approach is preferred. In this proposed comparator the energy recovering logic reuses charge and therefore consumes less power than non energy recovering logic [9]. Energy loss is an important consideration in digital design. Part of the problem of energy dissipation is related to non ideality of switches and materials [10]. The circuit consists of one XNOR realized by 4 transistors shown in fig 6. To illustrate static energy recovery considering an example where initially A=B=0 and then a charge to 1 [11]. When A and B both are equal to 0 the capacitor is charged by VDD. In next stage where B reaches a high voltage level keeping a fixed at a low voltage level, the capacitor discharge through A, now some charged is store in A. Hence when A reaches a high voltage there is no need to charge it fully. So energy consumption is low here. In this circuit two AND gates have been used which is design by pass transistor logic [12]. These two AND gates consist four NMOS devices for A<B or A>B output.

The strength of signal is an almost is measured by how closely it approximates an ideal voltage source. The stronger signal, the more current it can source or sink [13]. The power supplies VDD and GND are the source of the strongest 1 and 0. An NMOS transistor is almost perfect switch when passing a 0, it will pass a strong 0. However NMOS transistor is imperfect at passing 1.

Semicustom is another way to create the design by NMOS and PMOS devices using cell generator provided by the cadence. We choose the MOS device as per our requirement and adjust width and length according to that. Here we use 45 nm technology to design 1-bit comparator using two different design logics.

![Fig. 5 Schematic of 1bit comparator using 10 MOS devices](image)

The advantage of this approach is to avoid any design rule error. Fig. 5 shows the Schematic design of 1bit comparator using 10 MOS devices, which uses the combination of 7 NMOS and 3 PMOS transistors to fulfill the truth table of 1-bit comparator.

IV. RESULT SIMULATION AND DISCUSSION

Simulation waveform of one bit comparator using conventional MOS devices is given in fig. 6.
Simulation waveform of one bit comparator using 10 MOS devices is given in fig. 7 as:

![Simulation waveform of 1 bit comparator using 10 MOS devices.](image)

**Fig. 7** Schematic simulation of 1 bit comparator using 10 MOS devices.

The comparative analysis between various types of comparators is shown in table 2. It is observed that required number of MOS is less in static energy recovery and pass transistor logic as compared to conventional gate level implementation. Here comparisons are based on the power consumption and propagation delay, considering the number of gates in conventional type and semi-custom design.

**TABLE 2: ANALYSIS AND COMPARISON OF DIFFERENT APPROACHES**

<table>
<thead>
<tr>
<th>Approach Type</th>
<th>Power (µWatt)</th>
<th>Delay (ps)</th>
<th>No of MOS Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional MOS Approach</td>
<td>7.27</td>
<td>6.05</td>
<td>20</td>
</tr>
<tr>
<td>Proposed Semi-Custom Approach</td>
<td>3.03</td>
<td>2.73</td>
<td>10</td>
</tr>
</tbody>
</table>

It is clear from Analysis and comparison table that the power consumption in conventional MOS approach is 74µW whereas the proposed MOS approach consumes only 30.3µW and delay in case of proposed MOS approach is almost half as compared to the conventional MOS approach. Also we observe here that by using less MOS transistor the area requirement is also minimizes. By considering all the above parameters we can say that the 10MOS approach is best for design of 1 bit comparator.

![Comparison of power, delay and number of MOS devices for different approaches.](image)

**Fig. 8** Comparison of power, delay and number of MOS devices for different approaches

**V. CONCLUSION**

An alternative 1 bit comparator design by energy recovery XNOR and PTL AND gate then the number of MOS device is reducing to half of their conventional MOS (gate level) approach. Here we have further compare the schematic simulation of conventional MOS device with semicustom 10-MOS approach of 1 bit comparator. It is clearly observed by our work that the power consumption value of conventional MOS approach is 7.27µW, whereas in 10 MOS approach we obtain the value of power consumption as 3.03µW. Another comparison is based on propagation delay, in which a delay of 6.05ps is obtained in case of conventional MOS approach; whereas 2.73ps value is achieved in our proposed 10 MOS approach. So it is clear from the analysis that less propagation delay and efficient power device can be obtained from proposed semi-custom 10MOS design.

**REFERENCES**


