Design and Implementation of T-Flip Flop using GDI Techniques

Ritesh Kumar Yadav  
M.E. Scholar  
Department of Electronics & Communication  
NITTTR, Chandigarh, UT, INDIA

Rajesh Mehra  
Associate Professor  
Department of Electronics & Communication  
NITTTR, Chandigarh, UT, INDIA

Abstract:
Gate diffusion input is a modern technology, which provides implementation of digital circuit design to reduce area of digital circuits, power consumption and delay while advancement low complexity of logic design. In this paper, a new Gate diffusion input (GDI) t-flip flop is intended according to the abstraction of t flip flop in which fewer numbers of transistors are acclimated as compared to conventional t flip flop and as well it uses lesser power and lesser delay. Simulation results on 45nm technology, which show that the proposed T-flip flop has, the less circuit design area and prorogation delay of 67.35% and consumption power is 57.43% in a power supply of 1 V.

Keywords- GDI, CMOS, high speed, low power t-flip flop.

I. Introduction

Wider use of storage memory system and sequential logic for modern electronics triggers an interest which is higher performance and less area executions for essential memory components [1]. In this circuit the output value depend on both the current values of the input as well as the previous input values. This circuit is frequently called cyclic logic circuit. Their execution critically affects cyclic time and they frequently represent the largest fraction of entire power. Hence there are significant interests for the improvement of rapid and small power Timing component circuits and the same in techniques to assess their concert. Preceding work in Timing components description has neglected to think about the impact of circuit loading on the virtual positioning of Timing component structures. These above mentioned works acclimated fixed, and about acutely large, output loads when analyze alternatives. Input drive was either accustomed to be ample or was not indicated. Bistable circuits exist two stable states speaking to logic-1 and logic-0 [1]. These incorporate

Amplification and positive feedback are the two fundamentals for the realization of bistable operation. In keeping with these basics a circuit can be assembled with the assist of two cross-coupled inverter as proven in Fig. 1. On this circuit There are two stable states in which state-0 is described by means of Q is same to 0 and Q’ is equal to 1 and nation-1 is described through Q is same to 1 and Q’ is equal to 0. In this way this circuit can hold 1 bit of data [2]. Toggle flip flop can be recognized by connecting together with the input of JK flip flop. For master slave inputs, this regularly implies, including some additional circuitry to both the master and the slave latch so that the synchronous inputs will dominate independent of the clock and other inputs. These inputs are regularly used to instate the condition of digital ICs at the time the power is initially connected. Normally, a set or reset input is required, yet from time to time both. Alternatively whilst the enter signal is given to a t-flip flop it offers an output signal to two distinct outputs [2]. This paper proposes a low electricity speedy t flip flop with the help of GDI techniques. This novel method proposes a new strategy for designing logical circuits in standard technologies of CMOS.

![Figure 1- A bistable circuit of cross coupled inverter](image-url)
II. Design Logic

T-flip-flop is a much simpler model of the JK-flip flop. Right here both inputs of JK- flip flop are linked collectively so they may be called a single input J-ok flip-flop [3]. When clock pulse is given to the flip-flop, the output to be toggled. The circuit symbol of t-flip flop is shown below in figure-2.

This circuit is defined as though T is equal to 0 the state will not change and if T is equal to one then the flip flop will alternate the state means toggle the state [3]. Below the logic diagram of t flip flop is shown in figure-3 with its characteristic table and excitation table.

Table-1 characteristic and excitation table of T-flip flop

<table>
<thead>
<tr>
<th>Characteristic table</th>
<th>Excitation table</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

This performance gives the characteristic equation:

\[ Q_{next} = T \oplus Q = T\overline{Q} + \overline{T}Q \]

Now there are four terminals in essential GDI cell; where G stands for common gate input of p type metal oxide semiconductor and n type metal oxide semiconductor as like as CMOS inverter, P stands for the external node of p type metal oxide semiconductor transistor, N stands for the external node of n type metal oxide semiconductor transistor and node D stands for common diffusion for both transistors [10]. Depending upon the circuit structure P, N and D can also be used as input and output ports. Below figure-5 shows the basic GDI cell.

It should be commented that not all the function are possible in the ordinary pull up network CMOS procedure yet can be effectively executed in twin well CMOS technologies [12]. Most of them, the functions are difficult which uses 6-12 transistors in CMOS, and also standard PTL usage, on the other hand, very simple GDI techniques uses only 2 transistors per function [4]. As seen above the GDI cell structure is not much similar as the current PTL systems. GDI cell structure has various significant features which improves the design complexity level, power dissipation, number of transistors and logic level swing [5]. Bellow table-2 indicates how distinctive design changes the P inputs, N and G in the fundamental GDI cell compare to various Boolean functions at the output D [5].
Table-2 logic functions for GDI cell for different input designs [6]

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>Out</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>'0'</td>
<td>B</td>
<td>A</td>
<td>( \overline{A}B )</td>
<td>F1</td>
</tr>
<tr>
<td>B</td>
<td>'1'</td>
<td>A</td>
<td>( A + B )</td>
<td>OR</td>
</tr>
<tr>
<td>'1'</td>
<td>B</td>
<td>A</td>
<td>( A + B )</td>
<td>AND</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>( \overline{A}B + AC )</td>
<td>MUX</td>
</tr>
<tr>
<td>'0'</td>
<td>'1'</td>
<td>A</td>
<td>( \overline{A} )</td>
<td>NOT</td>
</tr>
</tbody>
</table>

The main advantage of GDI function is:
1. Low power circuit style
2. Permits falling power consumption
3. Reducing propagation delay
4. Reducing space of digital circuit
5. Maintaining low complexes of logic styles [6].

**a. Conventional t flip flops**

As the operation of the t flip flop, if T is in stage “0”, does not change the state and if T is in stage “1”, the state will toggle. This t-flip flop based on conventional CMOS in a figure-5 uses forty eight (48) transistors and consumes additional power [11].

**b. t flip flop using the basic GDI technique**

In this, all gates are designed in light of GDI procedures. Where two (2) three inputs GDI AND gates are utilized, four (4) two input GDI NOR gates are utilized, and two (2) two input AND gates are utilized [3]. This circuit utilizes thirty (30) transistors as appeared in figure-6.

**c. t flip flop based on GDI multiplexer technique**

It comprises of Master-Slave connection of two GDI Latches and few gates are appeared in Figure-8. Every latch has four essential GDI cells, which results in a simple 8-transistor structure and gates have 6-transistors related to latch. By utilizing 2-transistor, GDI gate is prohibited by the Clock signal. A clock signal fed to the transistors gate and gives two distinctive states:
1. When the Clock signal is low and the signal is propagate during p-MOS transistors, makes a transient state.
2. When the Clock signal goes to high state and the previous values are kept up as a result of conduction of the outputs [7]. At that point GDI gate holds the state of the latch and the other gates of t flip flop are in inverting gates. They are responsible for keeping the corresponding values of the internal signals and the circuit outputs.
Note that the dimension of the p-channel transistor is more widespread than that of the n-channel transistor [8]. For the correct operation, this size difference is not required. Maybe, it somewhat makes up for the distinction in the mobility of n-channel and p-channel transistors. The effective mobility of n-channel transistors is somewhere around two and four times that of p-channel transistors. These inverters have an imperative part to swing restoration and enhanced driving capacities of the outputs. It’s buffering of the internal signal and makes suitable output current for driving of load. It contains 22 transistors.

III. Proposed GDI t Flip Flop

The Proposed Gate Diffusion Input (GDI) t Flip flop has two latch circuits. Below figure-8 and figure-9 shows the schematic and symbol of proposed GDI t flip flop.

![Figure-9: Schematic of proposed t Flip flop based on GDI technique.](image)

![Figure-10: Symbol of proposed t Flip flop based on GDI technique.](image)

The latches are categories by (a) GDI gate and (b) inverter. This two (2) transistor GDI gate is proscribed by a clock signal. Clock signals are connected transistors gates and give two distinct states: When clock signal is low then the signal passes through p-MOS transistor and creates impermanent state (2)

When clock signal is high state then n-MOS transistor is on and the previous values are in the same state because the output will be conducted and GDI gates holds the latch state [9]. In previous paper t flip flop uses five GDI gates while in proposed paper t-flip flop uses only three GDI, which are more efficient for power and required area. The proposed t flip flop based on GDI gates contains only sixteen (16) transistors.

VI. Simulation Results

Below figure-11 demonstrates the simulation in which first signal indicates clocked signal, the second signal indicates information signal, third signal indicates the output Q and fourth signal demonstrates the output Qbar signal of the t flip flop. Figure-12 and figure-13 demonstrates the area and a power comparison of various t flips flop has also table -3 demonstrate the comparison of proposed t flip flop and other method t flip flop.

![Figure-11: simulation result of proposed t Flip flop based on GDI technique.](image)
The structure of proposed circuit is basic and some gates to describe t flip flop, contains 16 transistors. An enhancement technique was enhanced for Gate Diffusion Input (GDI) t Flip Flop, supported on repeating transistor size, while objective a negligible PDP product. Performance comparisons with other t Flip Flop design techniques were appeared concerning to gate area, delay and power dissipation. Simulation results by using cadence virtuoso tool in 45nm technology, CMOS process show that the proposed t flip flop has the least propagation delay of 167.8 psec, consumption power is 184.6 µW is achieved in a 1 V power supply. From the accomplished result, it can be concluded that GDI technique is better innovation from other distinctive innovation.

**TABLE 3:** Comparison Table for Proposed GDI t Flip Flop and additional methods

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Circuit</th>
<th>Number of transistors</th>
<th>Power [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Proposed GDI t Flip Flop</td>
<td>16</td>
<td>0.024</td>
</tr>
<tr>
<td>2</td>
<td>t Flip Flop based on GDI Multiplexer [3]</td>
<td>22</td>
<td>0.083</td>
</tr>
<tr>
<td>3</td>
<td>t Flip Flop on based GDI gates [3]</td>
<td>30</td>
<td>0.423</td>
</tr>
<tr>
<td>4</td>
<td>t Flip Flop based on CMOS technique [3]</td>
<td>48</td>
<td>0.764</td>
</tr>
</tbody>
</table>

**Table 3 Performance comparisons of various t flip flops**

**V. Conclusion**

In this paper, we proposed a Gate Diffusion Input (GDI) t flip flop for low-power design was presented.

**REFERENCES**


**Authors:**

Ritesh Kumar Yadav is currently associated with Electronics and Communication Engineering Department of Vidya Bhavan College for Engineering
Technology, Kanpur, India since 2012. He is ME-Scholar at National Institute of Technical Teachers’ Training & Research, Chandigarh, India and received Bachelor of Technology from UP Technical University, Lucknow, India in 2012. He has three years of academic and research experience. He has one paper to his credit which is published in IEEE International Conference. His research areas are Digital Signal Processing and wireless communication.

Dr. Rajesh Mehra: Dr. Mehra is currently associated with Electronics and Communication Engineering Department of National Institute of Technical Teachers’ Training & Research, Chandigarh, India since 1996. He has received his Doctor of Philosophy in Engineering and Technology from Panjab University, Chandigarh, India in 2015. Dr. Mehra received his Master of Engineering from Panjab Univeristy, Chandigarh, India in 2008 and Bachelor of Technology from NIT, Jalandhar, India in 1994. Dr. Mehra has 20 years of academic and industry experience. He has more than 325 papers to his credit which are published in refereed International Journals and Conferences. Dr. Mehra has guided 75 ME thesis. He is also guiding 02 independent PhD scholars. He has also authored one book on PLC & SCADA. He has developed 06 video films in the area of VLSI Design. His research areas are Advanced Digital Signal Processing, VLSI Design, FPGA System Design, Embedded System Design, and Wireless & Mobile Communication. Dr. Mehra is member of IEEE and ISTE.