A Power and Area Efficient Design of an 8-Bit Priority Encoder using 45nm Technology

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Abstract – The previous priority encoder circuits which faced problems like race conditions and charge sharing are eliminated by the proposed Priority Encoder. The main objective of the paper is to compare the power consumption and area of an 8 bit priority encoder in Semi-custom and Full-custom design. The power consumption in full custom has significantly reduced by 1.06 µW and design area has been reduced by 12.5 µm². This paper shows improvement in design of the priority encoder up to 19.7% in power and 13.5% in area.

Keywords - Priority Encoder, VLSI, CMOS, Low power design, look ahead scheme

1. INTRODUCTION

Priority Encoders find their use mostly in all communication systems. Interrupts in processors and other applications are prioritized using priority encoders.

A set of electronic components and circuits placed on a single silicon plate or a wafer constitute an Integrated Circuit. The CMOS Technology as described by the Moore’s Law leads to continuous miniaturization and reduction in number of transistors in an Integrated Circuit[1]. The advantages of IC Technology are improved cost, performance and power consumption characteristics[2]. With the growth in IC technology, the manufacturers are aiming towards higher speed ICs consuming less power and smaller chips. The circuits nowadays operate on high frequencies, thereby increasing the noise in the systems. The VLSI technology enters the nanometre ranges and with the decrease in these ranges the technology wish to achieve good drivability and noise robustness[3]. Priority encoders are one of the major decision devices used whenever a single resource needs to be shared with many operations and a priority needs to be fixed for the utilization of these resources[4]. As the size of ICs are reducing with time and new VLSI technologies are being introduced, there are constant researches being carried out to produce area and power optimized ICs.

This work proposes design of a robust 8 bit priority encoder and discusses the comparison between fully custom and Semi-custom design using Static CMOS at 45nm technology. Matsushita and Intel launched the commercial use of 45nm technology in 2007. While the IBM, AMD and Samsung followed them in 2008. The concept of Priority Encoder is first described in Section II. In Section III, the schematic of a robust 8 bit Priority Encoder is described along with the equations. In Section IV, the transient analysis of the Priority Encoder is discussed. In Section V, the result analysis of the Priority Encoder is discussed. Finally in section VI we discuss the conclusion of the implementation held with the software.

II. CONCEPT OF PRIORITY ENCODER

An encoder circuit, outputs an encoded value based on the states of all the inputs to the encoder circuit[5]. A priority function added to an encoder leads to a priority encoder circuit. For a system, where suppose two interrupts, interrupt the system simultaneously, the interrupt to be serviced depends upon the interrupt precedence or interrupt priority. The priority encoder circuit plays its role while prioritizing the interrupt service[6]. The two basic priority Encoders encountered in digital circuits are:

A. 4-Bit Priority Encoder:

The truth table of a 4-bit priority encoder is described in Table 1.

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>D₈</td>
<td>D₇</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Table 1 Truth table of 4bit priority encoder

Here in the truth table ‘X’ denotes the don’t care condition. D₀-D₃ are 4 input bits to the encoder. Y₀ and Y₁ are the corresponding output bits of the encoder.
The ‘V’ bit denotes the valid bit, which is set to ‘1’ when one or more input is high. If all inputs are low, the ‘V’ bit is set to ‘0’. The higher the $i$ value in $D_i$ the higher is the priority of the input bit. For the logic diagram the Karnaugh map of $Y_0$ is drawn in Table 2.

Table 2 K-Map of $Y_0$

$Y_0 = D_2 + D_3$ \hspace{1cm} (1)

Similarly the Karnaugh map of $Y_1$ is drawn in Table 3.

Table 3 K-Map of $Y_1$

$Y_1 = D_2 + D_1(D_2)$ \hspace{1cm} (2)

And the ‘V’ bit is given by

$V = D_0 + D_1 + D_2 + D_3$ \hspace{1cm} (3)

The logic Diagram of the 4 bit priority encoder is drawn in Figure 1.

Figure 1 Logic Diagram of 4 bit Priority Encoder

B. 8-bit Priority Encoder:

The truth table of an 8-bit priority encoder is described in Table 4.

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_0$</td>
<td>$D_1$</td>
</tr>
<tr>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
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<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Table 4 Truth table of 8 bit priority encoder

Here in the truth table ‘X’ denotes the don’t care condition. $D_0$-$D_7$ are 4 input bits to the encoder. $Y_0$, $Y_1$ and $Y_2$ are the corresponding output bits of the encoder[7]. For the logic Diagram, the K-Map calculation of $Y_0$, $Y_1$ and $Y_2$ are:

$Y_0 = D_1 + D_3 + D_5 + D_7$ \hspace{1cm} (4)

$Y_1 = D_2 + D_3 + D_6 + D_7$ \hspace{1cm} (5)

$Y_2 = D_4 + D_5 + D_6 + D_7$ \hspace{1cm} (6)

The logic Diagram of the 8 bit priority encoder is drawn in Figure 2.

Figure 2 Logic Diagram of 8 bit Priority Encoder

And the corresponding block diagram in figure 3.
III. SCHEMATIC OF THE PRIORITY ENCODER

The output of the proposed Priority Encoder is \( O_i = I_i \cdot P_i \), where \( I_i \) represents corresponding input data and \( P_i \) represents priority token passed[8]. The general expression can be written as

\[
O_i = I_i \cdot I_{i+1} \cdot I_{i+2} \cdot I_{i+3} \cdots \cdots \cdot I_0 \quad (7)
\]

For the three-level look ahead structure as shown in figure 4 the equations that follow are

\[
O_0 = L' \cdot I_0 
\]
\[
O_1 = L' \cdot I_1 \cdot I_0 
\]
\[
O_2 = L' \cdot I_2 \cdot I_1 \cdot I_0 
\]
\[
O_3 = L' \cdot I_3 \cdot I_2 \cdot I_1 \cdot I_0 
\]
\[
L_{\text{inter}} = L' + I_0 + I_1 + I_2 + I_3 
\]
\[
O_4 = L'_{\text{inter}} \cdot I_4 
\]
\[
O_5 = L'_{\text{inter}} \cdot I_5 \cdot I_4 
\]
\[
O_6 = L'_{\text{inter}} \cdot I_6 \cdot I_5 \cdot I_4 
\]
\[
O_7 = L'_{\text{inter}} \cdot I_7 \cdot I_6 \cdot I_5 \cdot I_4 
\]

The circuit enters pre-discharge mode when clock becomes 0 and outputs are pre-discharged when \( L_{\text{inter}} = 0 \)[9]. The circuit enters the evaluation phase when clock becomes 1.

IV. TRANSIENT ANALYSIS OF PRIORITY ENCODER

![Figure 5 Transient Analysis of Priority Encoder](image)

Transient response of the circuit is as expected from the circuit. For each input corresponding output can be seen in figure 5.

V. RESULT ANALYSIS

For the 45nm technology the priority encoder in power consumption and area parameters are compared over the Semi-custom and Full-custom design. The results obtained are as shown in Table 5.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Semi-Custom design</th>
<th>Full Custom design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (µW)</td>
<td>5.38</td>
<td>4.32</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>92.4</td>
<td>79.9</td>
</tr>
</tbody>
</table>

![Figure 6 Graph comparing full-custom and semi-custom design parameters](image)

VI. CONCLUSION

The proposed circuit has been found to perform better than existing designs as circuit proves to be temperature sustainable and consumes significantly less power to achieve high performance. The power consumption in full custom design has been improved from 5.38 to 4.32 µW, whereas less area circuit has...
been proposed which is reduced from 92.4 to 79.9 µm². There is an improvement of 19.7% in power consumption and 13.5% in area.

REFERENCES


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