An Efficient Sense Amplifier for SRAM using Body Biasing

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Abstract— This paper proposes design of a low power sense amplifier. It is designed for the low power and delay of the circuit by using the variable threshold mos devices. Sense amplifiers are used in the memories to increase the speed for accessing data from different locations. So the speed of data read of SRAM is highly reliable on the design of sense amplifiers. The introduced circuit is tested under the various conditions of fast changing current to maximum and minimum value and then obtained results are analysed. The designed circuit results in the low power consumption of about 186µW and delay of .87ns with the area of 305.9875µm².

Keywords — voltage sense amplifier, current sense amplifier, static random access memory, delay, yield, process corners.

I. INTRODUCTION

For VLSI chip designs portable and low power consumption are major challenges. In every device SRAM memories are the important part for storing data. SRAM strongly impact the overall functioning of the system. And sense amplifiers are the main peripheral component of the SRAM memory design. Sense amplifiers define the robustness of bit-line sensing, power and it also affects the read speed [1]. A variety of sense amplifiers and are used in various applications [2].

The main function of sense amplifier is to sense the differential signal at bit line and its complimentary line. The performance of the sense amplifier is greatly affected by the input offset voltage. The use of current sense amplifiers has a number of benefits over voltage sensing amplifiers [3]. The VLSA has the advantages of a higher sensing speed and a smaller layout area as compared to CLSAs because it has fewer transistors. However, because the output nodes also serve as input nodes, the sense amplifier enable (SAE) signal needs to be carefully controlled. The CLSA does not have this drawback, because it uses separate input and output nodes [4]. In order to control the power consumption same pull-up pmos can be used for precharging and sensing [5]. Leakage is also an important parameter that comes into the consideration with the scaling of the technology. Some techniques like adaptive voltage level are used to control the leakage current which results in the low power dissipation [6]. To reduce leakage power many other techniques like dual-Vth, multi-Vth, transistor stacking and body biasing are used [7].

In this paper the power and delay are improved using the body bias concept. It is introduced to reduce the power consumption without the noise margin degradation. It utilizes the low threshold voltage of mos transistors in order to reduce the delay during the read cycle. In this paper a model of sense amplifier is proposed whose operation is examined under the various conditions of temperature and substrate potential. Different technologies are used to the sense amplifier in order to reduce leakage current and power consumption. The power consumed during write operation is large so charge recycling is done through BL pairs. Here the performance of SRAM is improved by reducing the bit line capacitance. If bit line is reduced the parasitic capacitance decreases during the read cycle[8]. SRAM design consisting of 7T basic cell structure and the multithreshold technique in conjunction with the low power memristors are used for the power saving and delay reduction. MTCMOS based 7T Memristor SRAM is better. Memristor consume less total power and leakage power [9]. GDI techniques and PTL hybridizing methods are also powerful techniques to reduce the power and leakage [10].

Once the design is made it is observed under the different conditions of temperature and changing current and voltage values. For this chip is tested under various process corners where it tested under various combination of fast and slow nmos and pmos respectively. The systems may be featured with the viterbi decoders for error correction if errors are introduced in the systems [11].

This paper is organised as follow. In the SectionII basic architecture and working of memory is explained. SectionIII looks for the schematic design of the sense amplifier. In section IV layout and results of the design are discussed. Section V measurement results are explained. Finally section VI describes the conclusion of the design.

II. ARCHITECTURE

Architecture of SRAM consist of various modules to complete the process of storing and retrieving the data. The Fig. 1 shows an example of the basic SRAM memory. Pre-charge circuits are used to charge the bit and bitbar lines before the read operation in order to avoid delay. Row decoder and column decoders select the particular memory cell.
The data to the memory is written through the data write circuits and read through the sense amplifier circuit. This memory architecture consist of a number of peripheral circuitry to complete the data storage. Each circuit consumes area and power and hence these also results to the total area and power consumption in the circuit. So each module is designed with the important consideration.

![Fig. 1 Basic SRAM Memory Architecture](image)

Each module of the architecture is designed with the VLSI tool by using the minimum layout area structure so that overall area and power consumption is less. SRAM occupy major area in the chip so its area should be minimized for the compact design of the chip.

### III. Sense Amplifier Design

To select a suitable SA the factors like sensing delay, power consumption and PDP must be considered. The sensing delay is defined as the time that rising SAE reaches half of vdd to the time that Vout reaches 90% of Vdd. Also the power consumption is the idle power in yhe idle period and sensing power in sensing period.

Total power = Standby power/leakage power +active power

\[ P = cv^2f + V_{dd}I_d \]

Power consumption also depends on the frequency of operation. More is the switching transients more will be the power consumed by the circuit.

![Fig. 1 Schematic of sense amplifier](image)

The proposed sense amplifier circuit consists of five NMOS and four PMOS transistors. This circuit is in sensing mode when input to SEN is high. The circuit performance is tested for the precharge mode and read mode. The circuit is precharged by giving low voltage at NM4 and a high voltage at b and b’. Due to this, MP2, MP3 transistors performs in linear region and all the remaining transistors are in cutoff region. So the output will follow the input voltage (1.8V). Now for the read mode SEN and b’ is kept at high potential and b is kept at low. Under this condition, transistors MN1, MP0, 1 and 4 are in cutoff region and MN0, 2, 3, 4 and MP2, 3 are in linear region. Hence the out will follow the input whereas the out’ is low.

### IV. Simulations and result

The circuit is simulated under the different values of substrate voltage in order to reduce the threshold voltage of the transistors. Capacitors of 1pf small values are also attached to the input and output line in order to store the charge of the capacitive bit lines. As the length of these lines increases the net capacitance also increases. For the low power consumption variable threshold cmos are used, but increase in lower threshold voltage leads to increased leakage hence more standby consumption. So appropriate value of threshold voltage is determined. The transistors with the low threshold values switch faster than the high value threshold transistors. Here Vdd 1.5v is applied to the circuit. The circuit is simulated using the 100Mhz frequency. Fig. 3 shows the input conditions of the circuit.

![Fig. 3 Biasing voltage at the input terminal of sense amplifier](image)

Fig. 4 is the layout for the one stage of the sense amplifier. Each devices in the layout are using the same L value but different W. Width of pmos transistors is kept double or more than it to match the mobility and speed of both the devices. By
changing the width in the layout design lead to change in the behavior of transistors. But large increase may lead to the area overhead.

Fig. 4 Layout of latch type sense amplifier

Fig. 5 and Fig. 6 show the simulation results of the proposed circuit. Results are shown for the pre-charge mode and read mode separately. In the pre-charge mode bit and bit’ lines are charged to achieve the metastable state. Pre-charging ensures that the charging and discharging of the capacitive bitlines do not take much time during the read and write operation. It do not discharge from zero to full vdd instead starts charging from the pre-charged level. It is observed that in read mode when sense enable signal is activated the circuit senses the input and amplifies it. But when it is not activated it passes the previous stored value to the output. The biasing voltages to the circuit components and w/l ratio determine the sensing speed and consumed power of the circuit.

Fig. 5 Transient behaviour of SA prechargemode

Fig. 6 Transient behaviour of SA in readmode

Fig. 7 DC response of the proposed SA

Fig. 8 Shows the power graph for the power at different values of dc values. It is observed that the power consumption of the circuit rises with increase in the dc value. It consumes 64.68mw at 1.65v dc input.

Fig. 8 Graph showing power consumption of the circuit

V. MEASUREMENT RESULTS

In this paper, a sense amplifier is designed using 180nm CMOS process and demonstrated. Design uses a combination of pmos and nmos devices. The circuit is designed for high sensitivity. Data is stored in the circuit during the write cycle and output data is loaded when sense enable is made high and WE signal is low. The circuit is operated for the frequency 100MHz and the voltage applied is 1.5V. The pulse amplitude is kept at 1.8V. The area for the single sense amplifier circuit is 305.9875 µm². The measured results are shown in the tableI

<table>
<thead>
<tr>
<th>Table I</th>
<th>Circuit Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180nm</td>
</tr>
<tr>
<td>No. Of devices</td>
<td>4pmos,5nmos</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>Vdd:1.5V Vnb:-1.2V Vpb:-2.2V</td>
</tr>
<tr>
<td>Area</td>
<td>305.9875µm²</td>
</tr>
<tr>
<td>Maximum clock frequency</td>
<td>100MHz</td>
</tr>
</tbody>
</table>
Performance comparison shows that the delay of the proposed design is less but the power consumed increases comparatively. But the system is faster than the previous circuit designs.

**Table II**

**Performance Comparison of Proposed Sense Amplifier**

<table>
<thead>
<tr>
<th>Design</th>
<th>Area</th>
<th>Capacitor</th>
<th>Design Node (μm)</th>
<th>Power (μW)</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed</td>
<td>9T</td>
<td>4(pf)</td>
<td>0.18</td>
<td>186</td>
<td>.87</td>
</tr>
<tr>
<td>[11]</td>
<td>13T</td>
<td>no</td>
<td>0.18</td>
<td>21.2</td>
<td>.70</td>
</tr>
<tr>
<td>[12]</td>
<td>14T</td>
<td>no</td>
<td>0.18</td>
<td>84</td>
<td>1.10</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

SRAM’s are the building block of today systems. In order to achieve efficient systems, architecture and circuit techniques are improved to decrease the SRAM energy consumption. In order to save energy consumption the voltage is scaled down to the sub-threshold voltage during the memory design. But the low voltage variation has a prominent effect in functionality and performance of the chip. So in order to increase the performance a body biased sensing scheme is used. The performance under various conditions of temperature and Vdd is provided and efficiency of the circuit is checked. The best design is selected for the layout. According to the measurements made to the circuit the output power consumed is 186μW and also delay is improved to .87ns. Hence small area and better power management make this circuit possible to use in complicated system with improved power management.

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REFERENCES