Investigation on Fin and Gate Line Edge Roughness Effects for Sub-22 nm Inversion-Mode and Junctionless FinFETs

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Abstract — In this paper we investigated the line edge roughness (LER) effects on the 22-nm and 14-nm inversion mode (IM) and junctionless (JL) FinFETs by TCAD simulation. We examined the gate LER (GLER) effects and the fin LER (FLER) effects on the device variability separately. The simulation results show that the GLER-induced device variations will increase as the channel length decrease as expectation; however, the FLER-induced device variations will decrease as the channel length decrease. Consequently, in the deep nanometer regime, GLER-induced device variations will be a major problem for FinFETs as far as LER effects are concerned. Besides, LER will cause larger variation on the threshold voltage of the JL FinFET than that of the IM FinFET.

Keywords — FinFET, inversion mode, junctionless, line edge roughness, variability.

I. INTRODUCTION

As MOSFETs keep scaling down, the device variability becomes a serious problem. The sources of device variability can be classified into two groups. One is called random or intrinsic variation, which is caused by the inherent stochastic phenomena associated with each device, like random dopant fluctuation (RDF) and line edge roughness (LER). The other is called systematic or extrinsic variation, which is caused by the process variations, like the variations on the gate oxide thickness (tox) and the gate length (Lg). Basically, the intrinsic variation draws more attention since it cannot be eliminated by improving the process stability. Although RDF has been recognized as one of the major sources of variability [1, 2], LER is still considered as a non-negligible source of variability for the devices with 22 nm or shorter gate length [3-6]. On the other hand, the FinFET structure was adopted in the 22 nm technology node because it shows the better immunity against both the short channel effects (SCEs) and the device variability [2, 7]. Besides, the junctionless (JL) devices were proposed which can avoid the difficulty of precisely controlling the doping profiles [8]. The variability of JL and conventional inversion-mode (IM) FinFETs has been studied [9-13], however, most of them were based on 2D TCAD simulation and focused on the fin LER (FLER) effects and a comprehensive investigation on the comparison of FLER effects and gate LER (GLER) effects for both IM and JL FinFETs is seldom seen. In this work, we examined the FLER and GLER effects on sub-22 nm JL and IM FinFETs by 3D TCAD simulation. The effects of different FLER and GLER rms amplitude (σ) on the JL and IM FinFETs with different gate length will be investigated.

II. DEVICE STRUCTURES AND SIMULATION APPROACH

Fig. 1(a) shows the simulated device structure which is the SOI FinFET with 22 or 14 nm gate length and 10 Å gate oxide (SiO2) thickness. The fin height and fin width are 20 and 10 nm, respectively. The channel doping concentration is p-type $10^{15}$ cm$^{-3}$ for the IM device as Fig. 1(b) and n-type $10^{19}$ cm$^{-3}$ for the JL device as Fig. 1(c). The doping concentration for source/drain (S/D) extension is n-type $10^{19}$ cm$^{-3}$ and the length of S/D extension is 5 nm. The ohmic contacts are added at the ends of S/D extension in our simulation. The gate material is n+ polysilicon. No work function adjustment was made in our simulation. Figs. 2(a) and 2(b) show the FinFETs with GLER and FLER, respectively. For the IM FinFET, the top-view p-n junction profiles between the channel region and the S/D extension region are assumed to be the same as the gate edge profiles. The p-n junctions of the simulated IM FinFETs are assumed to be abrupt. In this work, we simulate two LER rms amplitudes ($σ = 1$ or 2 nm) and the correlation length of LER is set to be 12.6 nm which is predicted in ITRS 2013 for 14-nm high-performance logic transistors. The sample size for studying the LER-induced variability is 100. After the device samples which are produced by Sentaurus Process 3D are ready [14], the device simulation was performed for each device sample by Sentaurus Device 3D [15]. We use the hydrodynamic (HD) model combined with the density gradient (DG) model for quantum corrections [15] to simulate the
Fig. 1 (a) Simulated SOI FinFETs which may be (b) inversion-mode (IM) device or (c) junctionless (JL) device.

Fig. 2. The top view of an IM FinFET with (a) gate LER and (b) fin LER. The gate length of the FinFET is 14 nm and the rms amplitude of LER is 1 nm.

device characteristics. The simulation results will be presented and discussed in the next section.

III. SIMULATION RESULTS AND DISCUSSION

Fig. 3 shows the $I_D-V_G$ curves of the simulated IM and JL FinFETs with $L_g = 22$ or 14 nm without LER appearing. Table I shows the values of the key device performance parameters of these devices. The definitions of the key device performance parameters are as the following. The threshold voltage ($V_T$) is determined by the constant current method under $V_D = 50$ mV with the current criterion of 1 $\mu$A. The on-state current ($I_{on}$) and off-state current ($I_{off}$) are defined as the drain current under the gate overdrive of 1 V and $-0.5$ V, respectively, with $V_D = 1$ V. The subthreshold swing ($SS$) is also determined under $V_D = 1$ V. From Table I, the threshold voltage of the JL FinFET is about 0.3 V lower than that of the IM FinFET for the same gate length. This is because that the turn-on of the JL device does not need the formation of the inversion layer and hence a lower $V_T$ occurs. The small $V_T$ roll-off as the gate length reduced from 22 nm to 14 nm for both the JL and IM FinFETs suggests the simulated FinFET structure has good immunity to SCEs. The IM FinFETs have larger $I_{on}$ and smaller

<table>
<thead>
<tr>
<th>$L_g$ (nm)</th>
<th>Inversion Mode (IM) $V_T$ (V)</th>
<th>Junctionless (JL) $V_T$ (V)</th>
<th>$I_{on}$ (mA)</th>
<th>$I_{off}$ (pA)</th>
<th>SS (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>-0.04</td>
<td>-0.07</td>
<td>71.6</td>
<td>0.22</td>
<td>72.4</td>
</tr>
<tr>
<td>14</td>
<td>-0.32</td>
<td>-0.38</td>
<td>77.2</td>
<td>6.1</td>
<td>90.3</td>
</tr>
<tr>
<td>22</td>
<td>-0.3</td>
<td>56.5</td>
<td>56.5</td>
<td>0.63</td>
<td>74.6</td>
</tr>
<tr>
<td>14</td>
<td>-0.38</td>
<td>61.7</td>
<td>61.7</td>
<td>11.1</td>
<td>92.2</td>
</tr>
</tbody>
</table>

$V_T$ extracted at $I_D = 1$ $\mu$A with $V_D = 50$ mV

$I_{on}$ extracted at $V_G - V_T = 1$ V with $V_D = 1$ V

$I_{off}$ extracted at $V_G - V_T = -0.5$ V with $V_D = 1$ V

SS extracted at $V_D = 1$ V
$I_{off}$ than those of the JL FinFETs. This can be attributed to that the conducting layer of the IM devices is closer to the gate/channel interface than the JL devices and hence the effective oxide thickness (EOT) of the IM devices would be smaller than the JL devices and smaller EOT implies superior gate control. Although the fin height and fin width of the simulated FinFETs are arbitrarily chosen to be 20 and 10 nm, respectively, the simulated devices show the acceptable device performance and are capable of evaluating the trends of LER-induced device variations.

Fig. 4 shows the $V_T$ variations ($\sigma V_T$) caused by FLER and GLER for the JL and IM FinFETs with different gate lengths ($L_g = 22$ or 14 nm) and different LER rms amplitudes ($\sigma = 1$ or 2 nm). The error bars shown in Figs. 4, 5 and 6 represent 95% confidence interval. Obviously, the IM FinFETs have smaller LER-induced $V_T$ variation than the JL FinFETs. Since the conduction of JL FinFETs is directly related to the geometry of the fin, the FLER will induce more $V_T$ variation on the JL FinFETs than the IM FinFETs whose conduction is determined by the inversion layer. Besides, GLER induces more $V_T$ variation on the JL FinFETs than the IM FinFETs since the IM FinFETs have thinner EOT and better immunity to SCEs. Another important finding is that as the gate length decreases, the GLER-induced $V_T$ variation increases; however, the FLER-induced $V_T$ variation decreases. Since the SCEs become worse as the gate length decreases, the GLER effects also become more significant as the gate length decreases. The GLER-induced $V_T$ variation is proportional to the SCEs as the RDF-induced $V_T$ variation behaves which was discussed in [16]. In contrast with the GLER effects, the FLER effects become less significant as the gate length decreases. Under the fixed LER correlation length (12.6 nm in this work), as the fin becomes shorter, the variation on fin width actually becomes mitigated. As a result, the FLER-induced $V_T$ variation decreases as the gate length decreases. Therefore, for $L_g = 22$ nm, FLER dominates the $V_T$ variation for both the IM and JL FinFETs; however, as $L_g$ reduces to 14 nm, GLER dominates the $V_T$ variation for the IM FinFETs and GLER induces almost the same $V_T$ variation as FLER does for the JL FinFETs.

Fig. 5 shows the relative $I_{off}$ variations ($\sigma I_{off}$ divided by the mean of $I_{off}$) caused by FLER and GLER for the JL and IM FinFETs with different gate lengths ($L_g = 22$ or 14 nm) and different LER rms amplitudes ($\sigma = 1$ or 2 nm). Similar to the $V_T$ variation, as the gate length decreases, the GLER-induced relative $I_{off}$ variation increases; however, the FLER-induced relative $I_{off}$ variation decreases. For the JL FinFETs, the FLER-induced relative $I_{off}$ variation is larger than that of the IM FinFETs, since the fin geometry impact on the JL FinFETs is larger than that on the IM FinFETs. For the IM FinFETs, GLER dominates the relative $I_{off}$ variation especially when $L_g$ reduces to 14 nm. However, for the JL FinFETs, FLER induces larger relative $I_{off}$ variation than GLER does when $L_g = 22$ nm but the GLER-induced relative $I_{off}$ variation becomes larger than the FLER-induced relative $I_{off}$ variation as $L_g$ reduces to 14 nm.

Fig. 6 shows the relative $I_{on}$ variations ($\sigma I_{on}$ divided by the mean of $I_{on}$) caused by FLER and GLER for the JL and IM FinFETs with different
TABLE II

THE QUANTITATIVE SUMMARY OF THE FLER AND GLER INDUCED VARIATIONS ON BOTH THE IM AND JL FINFETS WITH LG = 22 OR 14 NM

<table>
<thead>
<tr>
<th>Device</th>
<th>Lg (nm)</th>
<th>( \sigma V_T ) (mV)</th>
<th>( \alpha_{FLER}/\alpha_{OFF} ) (%)</th>
<th>( \alpha_{GLER}/\alpha_{ON} ) (%)</th>
<th>( \sigma V_T ) (mV)</th>
<th>( \alpha_{FLER}/\alpha_{OFF} ) (%)</th>
<th>( \alpha_{GLER}/\alpha_{ON} ) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>JL</td>
<td>22</td>
<td>16.1</td>
<td>44.5</td>
<td>8.7</td>
<td>5.1</td>
<td>29.1</td>
<td>2.6</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>13.0</td>
<td>29.9</td>
<td>5.7</td>
<td>13.6</td>
<td>43.0</td>
<td>4.0</td>
</tr>
<tr>
<td>change due to Lg reduction</td>
<td>– 3.1</td>
<td>– 14.6</td>
<td>– 3.0</td>
<td>± 8.5</td>
<td>± 13.9</td>
<td>± 1.4</td>
<td></td>
</tr>
<tr>
<td>IM</td>
<td>22</td>
<td>3.0</td>
<td>10.0</td>
<td>11.3</td>
<td>0.7</td>
<td>23.0</td>
<td>2.7</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>1.7</td>
<td>9.0</td>
<td>7.6</td>
<td>5.2</td>
<td>43.1</td>
<td>4.4</td>
</tr>
<tr>
<td>change due to Lg reduction</td>
<td>– 1.3</td>
<td>– 1.0</td>
<td>– 3.7</td>
<td>± 4.5</td>
<td>± 20.1</td>
<td>± 1.7</td>
<td></td>
</tr>
</tbody>
</table>

gate lengths \((L_g = 22 \text{ or } 14 \text{ nm})\) and different LER rms amplitudes \((\sigma = 1 \text{ or } 2 \text{ nm})\). FLER causes larger relative \( I_{on} \) variations than GLER does for both the IM and JL FinFETs. The FLER-induced relative \( I_{on} \) variation on the IM FinFETs is even larger than that on the JL FinFETs since the inversion layer of the IM FinFETs directly conforms to the fin edge profile. Consequently, unlike the \( V_T \) and \( I_{off} \) variations, the JL FinFETs have smaller LER-induced relative \( I_{on} \) variation than the IM FinFETs. As the gate length decreases, the GLER-induced relative \( I_{on} \) variation increases but the FLER-induced relative \( I_{on} \) variation decreases, just like the \( V_T \) and \( I_{off} \) variations behave. Since FLER dominates the relative \( I_{on} \) variation, the LER-induced relative \( I_{on} \) variation actually becomes smaller as the gate length decreases for both the IM and JL FinFETs.

Table II is the quantitative summary of the FLER and GLER induced variations on both the IM and JL FinFETs with \( L_g = 22 \text{ or } 14 \text{ nm} \) when LER rms amplitude equals 2 nm \((\sigma = 2 \text{ nm})\). We can verify that as the gate length decreases, the GLER-induced variations increase but the FLER-induced variations decrease. Besides, we can also confirm that the JL FinFETs have larger LER-induced \( V_T \) and relative \( I_{off} \) variations but smaller LER-induced relative \( I_{on} \) variation than the IM FinFETs. Note that the FLER and GLER effects can be considered independently and the total LER effect can be predicted by the root of the square sum of the FLER and GLER effects [12]. We had verified the independence between the FLER and GLER effects although the simulation results are not shown in this paper.

IV. CONCLUSIONS

The FLER and GLER induced variations on the sub-22 nm JL and IM FinFETs have been simulated by 3D TCAD tools. Our simulation results show that as the gate length decreases, the GLER-induced variations increase but the FLER-induced variations decrease. Besides, we also found that the JL FinFETs have larger LER-induced \( V_T \) and relative \( I_{off} \) variations but smaller LER-induced relative \( I_{on} \) variation than the IM FinFETs. Lastly, we found that the LER-induced relative \( I_{on} \) variation actually becomes smaller as the gate length decreases for both the IM and JL FinFETs.

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REFERENCES


