Common Mode Voltage Reduction in DCMLI

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Abstract: This paper presents modulation strategies to reduce common mode voltage in diode clamped multilevel inverter. During operation of diode clamped inverter it produces common voltage which is not zero, this causes significant impact on the motor. The carrier pulse width modulation strategies are implemented for five level diode clamped multilevel inverter and the variation of common mode voltage is observed and presented using SIMULINK.

Keywords: common mode voltage, diode clamped, carriers pwm

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975 [1]. The term multilevel began with the three-level converter [2]. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation.

II. COMMON MODE VOLTAGE

CMV is defined as the voltage at the star point of the load and the system ground. The magnitude of the CMV depends on grounding system [1]

\[ V_{\text{com}} = \frac{1}{3}(V_a + V_b + V_c) \]  

Because of 12 switches in the Neutral Point Clamped or Diode clamped inverter shown in Fig. 1, they produce 19 output voltage vectors including a zero voltage vector. If sum of the output voltages is not zero, a common-mode voltage results. An example of waveforms of phase voltages and the resulting common-mode voltages are shown in Fig. 2.

\[ V_a = V \sin(wt) + V_{np} \]
\[ V_b = V \sin(wt-120^\circ) + V_{np} \]
\[ V_c = V \sin(wt-120^\circ) + V_{np} \]
Finally, the NP voltage variations generate common-mode voltage at three times the fundamental output frequency, which occurs even if the high frequency and high dv/dt switching common-mode voltage is mitigated by some techniques such as filtering. When the common-mode voltage and resulting shaft voltage caused by the NP voltage variation are large enough to break the oil film insulation in the bearings, bearing currents are generated, which by erosion may cause premature failures of the motor bearings. Hence the NP voltage control is important not only for the Neutral Point Clamped or Diode Clamped inverter operation but also for common-mode voltage mitigation [2]. The shaft voltage is measured between the motor shaft and the motor frame, which is usually grounded. It is generated by the common-mode voltage coupling through the path that consists of the motor stator windings, rotor windings and the distributed capacitance between them. Its magnitude is dependent on not only the magnitudes of the common-mode voltage but also the coupling impedance[6].

III. MULTICARRIERPULSE WITH MODULATION

This section of the chapter extends the principles of carrier-based PWM that are used for multilevel inverter. There are three alternative PWM strategies with differing phase relationships:

3.1 Phase Disposition (PD)

3.2 Phase Opposition Disposition (POD)

3.3 Alternative Phase Opposition Disposition (APOD)

3.1 PHASE DISPOSITION PWM (PDPWM)

The carriers are in phase across all the bands. The zero reference is placed in the middle of the carrier sets. For this technique, significant harmonic energy is concentrated at the carrier frequency, but since it is a cophasal component, it doesn’t appear in the line-to-line voltage.

Fig.3 Comparison of reference wave and phase disposition carrier waves for five level

**Phase Opposition Disposition Pwm**

All the carriers above the zero reference are in phase and carriers below the zero reference are also in phase but are phase shifted by 180° with respect to that above zero reference. The significant harmonics are located around the carrier frequency, for both the phase and line-to-line voltage waveform.

Fig.4 Comparison of reference wave and phase opposition disposition carrier waves for five level

**ALTERNATE PHASE OPPOSITION DISPOSITION**

Carriers in adjacent bands are phase displaced by 180°. With this method, the most significant harmonics are centered as side bands around the carrier.
IV. SIMULATION RESULTS

Fig. 5 Comparison of reference wave and alternate phase opposition disposition carrier waves for five level

Fig. 6 Three phase line voltages of five level DCMLI

Fig. 7 Common mode voltage for phase disposition scheme

Fig. 8 Three phase line voltages of five level DCMLI

Fig. 9 Common mode voltage for phase opposition disposition scheme

Fig. 8 Three phase line voltages of five level DCMLI
V. CONCLUSION

In this paper five level diode clamped multilevel inverter is simulated by SIMULINK. The different pulse width modulation strategies like phase disposition, phase opposition disposition, alternate phase opposition disposition are implemented for these five level diode clamped mli. The common voltage is reduced by these techniques and supported by Simulink results.

REFERENCES