Achieving Power and Area Reduction by Redesigning Existing Memory IC

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Abstract—With increase in complexity and shrinking technology below 100 nm, reducing power consumption and over all power management on chip are the key challenges. Multi-bit flip-flop is an effective method for clock power consumption reduction proven by the researchers. By sharing the inverters in the flip-flops, the total number of inverters can be reduced in a multi-bit flip-flop. So, here, in this paper we have redesigned the internal circuitry of an IC which is an important memory element in digital systems, using 4-bit and 8-bit flip flop. Experimental results show that our approach is very efficient in reducing its area and power consumption, and hence will be very useful in modern vlsi circuit designs.

Keywords— sub-micron, drive strength, master slave, multi bit flip flop, merger.

I. INTRODUCTION

Earlier, the two main things— increasing the speed and reducing the area of digital systems have been the main focus points of the digital system designers. But now, with the evolution of portable systems and advanced deep Sub-Micron fabrication technologies, power dissipation has become another critical design factor. As the low power design reduces cooling cost and thus increases the reliability especially for high density systems. Also, the lower power consumption requirement continues to increase significantly because the components have become smaller, require more functionality and battery-powered.[2]

For VLSI chips flip-flop is a basic and important building circuit. [4]If larger multi-bit flip-flops are used in place of smaller single bit flip-flops, device variations in the corresponding circuit can be effectively reduced. Multi bit flip flop is a cluster of many single-bit flip-flops i.e. they share the drive strength. So, the use of multi-bit flip-flops can reduce clock circuitry and power consumption as well.

II. MULTI-BIT FLIP FLOP

Given below is the schematic of the technique of merger of two 1-bit flip-flops into one 2-bit flip-flop (fig. 1).

Fig. 1 Method of merging two 1-bit flip-flops into one 2-bit flip-flop.

So, we can see that common clock is being provided to the multi bit flip flop circuit. Hence, by merging single-bit flip-
flops into one multi-bit flip-flop, the duplication of inverters can be avoided. So, by using this concept we designed 4-bit and 8-bit D flip flops. Here is the block diagram of 4-bit flip flop.

![Fig. 2 Block Diagram showing 4-bit D flip flop.](image)

The output waveform for the 4-bit D flip flop is as given below:

![Fig 3. Simulation result of 4-bit flip flop.](image)

The block Diagram for 8-bit D flip flop is generated using Xilinx software.

![Fig 4. Block Diagram showing 8-bit D flip flop.](image)

Here are the simulation results for multi bit flip flop.

### III. CONVENTIONAL IC 4731B

The 4731B is a CMOS quad 64-bit shift register. It contains four identical 64-bit shift registers on one chip. So, here we are taking one of the 64-bit registers. It has a serial input, a clock input and a serial output from the last flip flop. This is the only output that is externally accessible. All flip flops are master-slave flip flops. Master slave flip flop is also called pulse triggered flip flop.

Master flip flop is triggered when clock=1 and slave flip flop is triggered when clock =0 and slave copies the master. The information from inputs is transferred to master flip-flop at positive/leading edge of the clock pulse and slave flip-flop remains disabled. A negative/trailing edge information is transferred at the output of slave and master remain disabled. The output of master-slave flip-flop changes only at the end of clock pulse and race around condition never occurs. The slave just copies the master. Since output of the master slave changes only after arrival of complete pulse, that is why it is also called pulse triggered flip flop.
The cadence generated internal diagram of 4731B is as given:

IV. PROPOSED DESIGN USING 4 BIT D-FLIP-FLOP:

Instead of using conventional D flip flops. In this section, we will introduce how to design a shift register using multi-bit flip-flop. Since we want to replace the single bit flip-flops with multi-bit flip-flop that must have identical clock conditions and similar type of logic levels to set or reset the flip flops.

Fig. 8 Block Diagram using 4-bit D flip flops.

We employed the concept of multi bit flip flop in designing a shift register used in this digital system. By using multibit flip flop we are able to reduce the total power consumption of the circuit and hence is very advantageous.

Fig. 7 Internal Circuitry of 4731B.

Fig. 9 Cadence generated internal circuitry.

The output waveform is as shown:

Fig. 10 Output waveform.

V. DESIGN USING 8-BIT D FLIP-FLOP:

Extending the concept further we used 8-bit master slave D flip flops, we are able to further reduce the power consumption of the circuit. So, the block diagram is as shown:
From the power analysis table it is clear that by employing 4-bit D flip flop and 8-bit D flip flop there is a reduction of 10.28% and 11.43% in the total power respectively. Also, there is significant reduction in area as well. With 4-bit D flip flop and 8-bit D flip flop the total area on IC is reduced by 12.66% and 14.13% respectively. Hence it is clear that our approach is very efficient in area and power reduction.

VIII. CONCLUSION

We implemented the concept of 4-bit and 8-bit D flip flop in redesigning the constituent stages of an integrated circuit with which we are able to effectively reduce the area and power consumption of the circuit. The Simulated waveforms of the resultant circuit are the same as that of the original integrated circuit. We carried out the implementation using cadence and Xilinx software. The schematic and waveforms are given in the paper. This basic concept of multi-bit flip flop can be extended to the design of other sequential circuits in future.

VI. POWER AND AREA ANALYSIS

TABLE I

<table>
<thead>
<tr>
<th>S. No.</th>
<th>IC 4731B Using</th>
<th>Leakage Power(nW)</th>
<th>Dynamic Power(nW)</th>
<th>Total Power(nW)</th>
</tr>
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<tbody>
<tr>
<td>1.</td>
<td>1-bit D flip flop</td>
<td>457.389</td>
<td>273430.625</td>
<td>273888.014</td>
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<tr>
<td>2.</td>
<td>4-bit D flip flop</td>
<td>441.674</td>
<td>245270.016</td>
<td>245711.690</td>
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<tr>
<td>3.</td>
<td>8-bit D flip flop</td>
<td>439.852</td>
<td>242136.964</td>
<td>242576.816</td>
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</table>

TABLE II

<table>
<thead>
<tr>
<th>S. No.</th>
<th>IC 4731B Using</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>1-bit D flip flop</td>
<td>12688</td>
</tr>
<tr>
<td>2.</td>
<td>4-bit D flip flop</td>
<td>11082</td>
</tr>
<tr>
<td>3.</td>
<td>8-bit D flip flop</td>
<td>10895</td>
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REFERENCES


