Area Efficient Low Power Vedic Multiplier Design Using GDI Technique

Nidhi Pokhriyal[#1], Neelam Rup Prakash[*2]

[#1]*ME Research scholar, EC Department, PEC University of Technology*

[*2]*Supervisor, EC Department, PEC University of Technology*

***Abstract*—Multipliers consume maximum amount of power during the partial product addition. For higher order multiplication, a huge number of adders are used to perform the partial product addition. Using compressor adders, that can add four, five , six or seven bits at a time, the number of full adders and half adders can be reduced and thus area and power consumed also gets reduced. These compressor adders are designed by merging binary counter property with compressor property. In this paper, transistor level implementation of a Vedic multiplier based on a Vedic sutra, Urdhva Tiryakbhyam, is proposed. Higher order compressors are used in partial product addition stage to get the final result. A power efficient technique, Gate Diffusion input, has been used to design all the leaf cells of the multiplier. The designs are synthesized and analysed using Cadence Virtuoso tool in 180nm technology. When compared with CMOS based multiplier, the proposed multiplier shows 36.05% reduction in area and 31% reduction in power.**

Keywords—**Compressor, Gate diffusion input technique, multiplier, binary counter, low-power.**

I. INTRODUCTION

Multipliers have an important effect in designing arithmetic, signal and image processors. Many important functions in such processors make use of multipliers. Many current DSP applications are targeted at portable, battery-operated systems, due to which power dissipation becomes one of the primary design constraints.

The multiplier is generally the slowest element in the system hence system's performance is generally determined by the performance of the multiplier. At the same time, multipliers are the most area consuming elements in the system. Power dissipation in a multiplier is a very important issue as it shows the total power dissipated by the device. Hence it affects the device's overall performance.

As multipliers are the main component of many handheld devices, the power requirements are more stringent for them. Hence there is a requirement of efficient low power and low area multipliers.

A multiplier is typically composed of three stages –partial product generation stage, partial product addition stage and final addition stage.

In the first stage, multiplicand and multiplier are multiplied bit by bit to generate partial products. The second stage is the most important stage as it is the most complicated and determines the speed and power consumption of overall multiplier. The addition of the partial products contributes most to the overall delay , area and power consumption due to which the demand of high speed and low power adders is continuously increasing.

Compressor adders have been widely employed in many high speed power and area efficient multipliers [1][2][3]. In the partial product addition stage, compressors contribute to the reduction of the partial products by reducing the number of adders at the final stage and also contribute to the reduction of critical path which is important to maintain the circuit's performance. Top level designs of compressors are presented in [1]

Conventional CMOS design technique is best in terms of output logic level. Both logic-1 and logic-0 are transferred correctly at the output but at the expense of large area and high power consumption.

In CMOS circuits, power dissipation primarily occurs during device switching. Whenever input signal rises or falls, a very large current starts flowing suddenly between VDD and GND. This large current leads to very high power consumption. In order to reduce to power dissipation and area, Gate diffusion input technique is used in compressor designs presented in this paper.

Section II describes Urdhwa Tiryakbhyam Sutra for 8-bit multiplication. Section III deals with the compressor basics. Section IV deals with the Gate diffusion input technique in detail. Section V describes the multiplier design implemented using GDI technique. Section VI deals with the performance evaluation and results. Section VII deals with the conclusion and future work.

II. VEDIC SUTRA - URDHWA TIRYAKBHYAM

The 16 Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Among these sutras, Urdhwa Tiryakbhyam Sutra is the most efficient for performing multiplication.

The use of this sutra can be extended to binary multiplication as well .This Sutra translates to "Vertical and crosswise". It utilizes only logical AND operation, half adders and full adders to perform

multiplication where the partial products are generated prior to actual multiplication. This saves a considerable amount of processing time. Moreover it is a robust method of multiplication.

Consider two 8-bit numbers, a (a8-a1) and b (b8-b1) where 1 to 8 represents bits from the least significant bit to the most significant bit. The final product is represented by P (P16-P1). In Fig.1, the step by step method of multiplication of two 8-bit numbers using Urdhwa Tiryakbhyam Sutra is illustrated. The bits of the multiplier and multiplicand are represented by dots and the two way arrow represents the logical AND operation between the bits which gives the partial product terms.

In the conventional design of Urdhwa Tiryakbhyam sutra based multiplier, only full-adders and half-adders are used for addition of the partial products. But, the capability of full-adder is limited to addition of only 3 bits at a time.

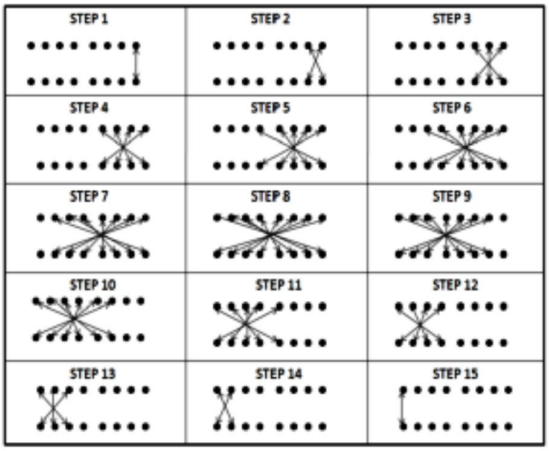

Fig.1. 8-bit binary multiplication using Urdhwa Tiryakbhyam Sutra

Large number of stages is required to get the final result of addition if conventional adders are used. Hence to reduce the numbers of stages, higher order compressor are to be used.

III. Compressor basics

Compressors are major components of the present multiplier designs. Compressor adders are formed by combining the property of a binary counter with that of a compressor. In multipliers maximum amount of power is consumed during the partial product addition. For higher order multiplication, a huge number of adders or compressors are used to perform the partial product addition. Using compressor adders, which can add four, five, six or seven bits at a time, the number of full adders and half adders can be reduced. In the present work 4:3, 5:3, 6;3, and 7:3 compressors are used .

IV. Gate diffusion input technique

Using GDI technique, implementation of a wide range of complex logic functions is possible using only two transistors. GDI technique is based on the use of a simple cell which looks like standard CMOS inverter as shown in fig.2, but there are some important differences [4]

(1) GDI cell consists of 3 inputs. G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS) and N (input to the source/drain of nMOS).
(2) N or P (respectively) are connected to bulks of both nMOS and pMOS, so it's biasing can be done arbitrarily at contrast with CMOS inverter.

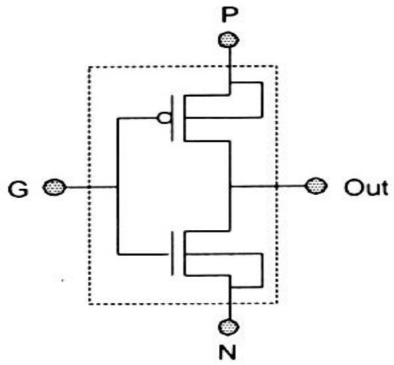

Fig. 2. Basic GDI cell

GDI technique is suitable for design of efficient low-power circuits. It uses a reduced number of transistors as compared to CMOS. At the same time, it improves logic level swing and static power characteristics and allows simple top-down design by using small cell library.

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions [4].

TABLE I

FUNCTIONS IMPLEMENTED USING GDI TECHNIQUE

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

These functions are very complex when implemented in CMOS logic and require 6-12 transistors. But the same functions are very easy to implement using GDI method and require only two transistors per function.

Here one important thing to be noted is that all the functions are possible in standard p-well CMOS process but can only be successfully implemented in twin-well CMOS or SOI technologies. Both F1 and F2 form complete logic families. They allow realization of any possible two-input logic function. But F1 is the only GDI function that can be

realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased.

When N input is at high logic level and P input is at low logic level, the diodes between NMOS and PMOS bulks to Out are directly polarized and there is a short between N and P which results in static power dissipation and Vout~0.5 VDD. This is a drawback for OR, AND, and MUX implementations in regular CMOS with V_{BS}=0 configuration. The effect can be reduced if the design is implemented in floating-bulk SOI technologies [5], where a full GDI library can be implemented. But here, floating-bulk effects have to be considered.

TABLE II

TRANSISTOR COUNT COMPARISON

Circuit	Transistor Count	
	GDI Technique	**CMOS Technique**
4:3 Compressor	88	132
5:3 Compressor	98	156
6:3 Compressor	108	180
7:3 compressor	206	318
Multiplier	2394	3744

V. PROPOSED MULTIPLIER DESIGN

The complete multiplier design can divided into two stages:

1. Partial product generation
2. Partial product addition

Transistor level implementation of a Vedic multiplier design is done using Gate Diffusion input technique. Partial products are generated and arranged according to Urdhva Tiryakbhyam sutra. Then for addition of partial products, higher order compressors are used. At the final stage of addition, carry look ahead adders are used. All the leaf cells are designed at transistor level using GDI technique.

The multiplier design is done at transistor level using Cadence Virtuoso tool in 180nm technology. Figure 3 shows the transistor level implementation of complete design of the multiplier. All the leaf cells of the design, compressors are designed using GDI technique.

Figure 4 shows the output waveform of the designed multiplier.

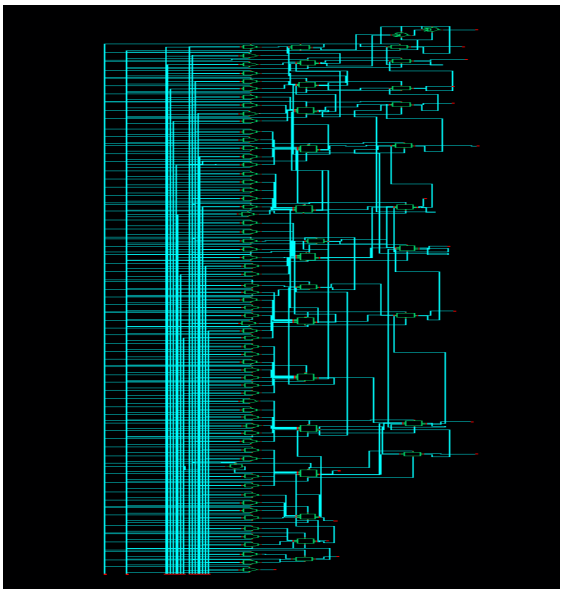

Fig. 3 Transistor level implementation of proposed multiplier

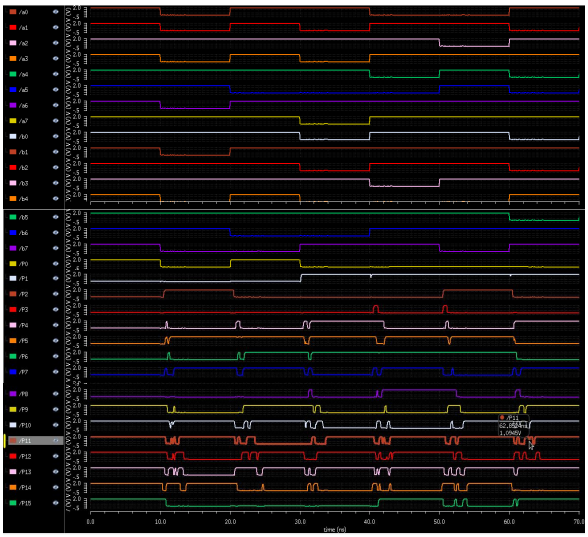

Fig 4. Output waveform of proposed multiplier

VI. PERFORMANCE EVALUATION AND COMPARISON

The Vedic multiplier designed using GDI technique is compared in terms of area and power with Vedic multiplier designed using CMOS technique. Table II shows the transistor count comparison for compressors and multiplier. This comparison shows that the multiplier implemented using GDI technique uses less transistor than that implemented with CMOS technique. Thus we see that the multiplier implemented with GDI technique occupies much less area than the CMOS multiplier.

As with the use of GDI technique, number of transistor is reduced, the total power consumed is also reduced. Table III shows the power consumption comparison for compressors and multiplier. It clearly shows that the multiplier implemented using GDI technique consumes less power than that implemented using CMOS technique.

TABLE III
TRANSISTOR COUNT COMPARISON

Circuit	Total Power Consumption (mW)	
	GDI Technique	CMOS Technique
4:3 Compressor	1.159	2.478
5:3 Compressor	2.098	5.484
6:3 Compressor	2.168	6.242
7:3 compressor	3.006	6.254
Multiplier	14.33	20.76

VII. CONCLUSION

A multiplier based on the Urdhva Tiryakbhyam sutra of ancient Vedic Mathematics is implemented. In the partial product generation stage compressor adders are used. All the leaf cells are designed using power efficient Gate diffusion input technique. Multiplier is implemented in Cadence Virtuoso tool using 180nm technology. The simulation of the designed multiplier is done using 1.8 volt supply voltage and compared with CMOS implementation of the same multiplier. We observed that the multiplier implemented using GDI technique uses less number of transistors than its corresponding CMOS implementation. Also the power consumption in the GDI cell based multiplier is very much less than for the CMOS implementation. The multiplier designed using GDI technique shows 36.05% improvement in area and 30.97% improvement in power consumption when compared with the CMOS multiplier.

As the future scope of the work, the power of the circuit can be further reduced by sizing the transistor keeping logical effort in mind. We can consider the GDI technique in sequential logic designs and mixed circuits.

We can also use this technique with the other low power design methods. The proposed multiplier is implemented using the standard p-well CMOS process, which poses the limitation on a GDI cell library. Still even in limited-library-based GDI circuits, significant improvement in area and power consumption is observed. Implementation of GDI circuits in SOI or twin-well processes are expected to give more power and area efficient designs.

REFERENCES

[1] A Dandapat, S. Ghosal, P. Sarkar. & D. Mukhopadhyay, 2010. A 1.2-ns16×16-Bit Binary Multiplier Using High Speed Compressors. *World Academy of Science, Engineering and Technology*, Volume 4, pp. 556-561

[2] S. R. Huddar, Kalpana M, surbhi Mohan ,Novel High Speed Vedic Mathematics Multiplier using Compressors, *Confererence proceedings of IEEE,2013*

[3] N.Pokhriyal, H. Kaur, H. & D. N. R Prakash,. 2013. Compressor Based Area-Efficient Low-Power 8x8 Vedic Multiplier. *Int. Journal of Engineering esearch and Applications*, 3(6), pp. 1469-1472.

[4] Arkadiy Morgenstern, Alexander Fish and Israel A. Wagner, GATE-DIFFUSION INPUT (GDI) – A technique for low power design of digital circuitsAnalysis and characterization, *IEEE proceedings of circuits and systems*, 2002

[5] I. Sutherland, B. Sproull, and D. Harris, *Logical Effort: Designing Fast CMOS Circuits*. San Mateo, CA: Morgan Kaufmann, p. 7.