Performance Analysis and Synchronization Failures in Deep sub Micron Technology

Ambresh Patel¹, Anand Kumar Singh², Sachin Bandewar³

¹,²,³Electronics & Communication Engineering Department, Sri Satya Sai College of Engineering, Bhopal, India

Abstract- Synchronizers were required when reading an asynchronous input. In a multi clock system, synchronizers are required when on-chip data cross the clock domain boundaries which guard against synchronization failures but introduce latency in processing the asynchronous input. We use method that hides synchronization latency by overlapping it with computation cycles. Synchronization time can be reduced by using faster flip-flops and produces a transition whose clock-to-q delay is longer than expected, this transition may not have sufficient time to reach all destination flip-flops.

Keywords—Setup Time, Hold Time, Soft errors, Flip-Flops, Synchronization Failure, Metastability.

I. INTRODUCTION

The crossing of data between different clock domains requires re-timing the data according to the receiver’s clock and is prone to synchronization failures. While it is impossible to completely prevent these failures, their probability can be reduced to an acceptable level by re-sampling the input signal through a cascade of flip-flops known as a synchronizer. This ensures that any occurrences of metastability are given enough time to resolve to valid logic states before being interpreted by other circuits. Metastability is another growing concern, especially as frequencies increase and timing margins are shrunk in contemporary chips. It is a phenomenon where the bi-stable element such as flip-flop enters an undesirable third state in which the output is at an intermediate level between logic “0” and “1.”

II. LITERATURE REVIEW

Ghaith Tarawneh work on synchronization failure in latches and flip-flops. In synchronizer circuits, metastability failures introduce latency in processing the asynchronous input. Synchronization time can be reduced by using faster flip-flops. The state of a synchronizer can be used to sequence a series of latching operations correctly. This is done by making the satisfaction of the setup conditions of all the paths from the synchronizer flip-flops to the data registers a necessary condition for a change in the synchronizer state [1]. Metastability is the inability of a latched comparator to reach a decision in the available amount of time. Existing analyses of metastability disregard noise, treating it as a deterministic phenomenon that inevitably happens every-time the input voltage, Vidiff, falls in a certain interval around 0, and which is restricted to the aforementioned interval. Also, according to the conventional analysis, the decision takes an infinite amount of time if Vidiff=0 [2].

Synchronization failure can eliminate by many researchers using one clock, faster flip-flops, decrease the asynchronous input frequency, and use synchronization hardware.

David Rennie, David Li, Manoj Sachdev, Bharat L. Bhuva uses synchronize flip-flops. The first flip-flop is a standard master slave flip-flop, which is used as a reference flip-flop. The second flip-flop replaces the master and slave storage cells with the Quatro cell. The third and fourth flip-flops have only the slave stage protected, in one case with the DICE cell and in the other case with the Quatro cell. In all cases tri-state inverters are utilized as transfer gates. In this work they propose the metastability detector circuit with error detector circuit and error counter. The difference between the clock arrival time at error detector circuit detects metastability event which counted by error counter [3].

David J. Rennie, and Manoj Sachdev design a test chip was implemented in nanometer process. They also design second hardened storage cell which can be used is the eight transistor Quatro cell. They work on transmission gate base master slave flip-flops. By combining different transfer gates with the Quatro latch, a variety of flip-flops can be realized. The transfer gate provides a mechanism for controlling the flow of data into the storage cells while the storage cell stores the data after the transfer gate is deactivated [5].

Keith A. Bowman, James W. Tschanz, Nam Sung Kim, Janice C. Lee work on a 65 nm Energy-Efficient and Metastability-Immune Resilient circuits with error detection and
recovery logic to monitor timing faults for online testing of digital circuits [7]. Antonio Cantoni, Jacqueline Walker, and Toby-Daniel Tomlin develop an equation describing the time interval between data and clock inputs for practical frequencies and show that it takes on discrete values in the absence of jitter and that the presence of jitter perturbs these values. Their analysis in asynchronous input is not uniformly distributed around the clock edge but instead occupies discrete time instants, where an asynchronous data input and clock are used to trigger synchronization failure in a bistable device [8].

III. TIMING DELAY ANALYSIS

(a) PROPAGATION DELAY

The propagation delay of a flip-flop is defined as its clock-to-output delay. This equals the maximum delay from the arrival of the clock’s active edge to the output of the flip-flop is considered stable. Usually the propagation delay differs from low to high transition and high to low transition.

(b) SETUP TIME

The setup time is defined as the time the data value must remain stable around the arrival of the clock’s active edge to ensure that the flip-flop retains the proper output value. Synchronous machines are clocked at a fixed rate. At every clock edge, a subset of the machine’s state bits are changed and the transitions of these bits propagate through series of logic gates (i.e. combinational logic paths) back to the state register inputs. The clock period must be long enough to let this process complete before the following clock edge. This is referred to as the setup time condition and must be satisfied for all the combinational paths between the machine’s flip-flops. The setup condition of a path between two flip-flops FF1 and FF2 can be expressed as: 

tclk-q + tpd + tsu + tskew < T

where tclk-q is the time between the occurrence of a clock edge and the availability of the latched value on FF1’s output (this is referred to as the clock-to-q delay of the flip-flop), tpd is the propagation delay of the path FF1!FF2 (the sum of all gate and interconnect delays on this path), tsu is the setup time of FF2, tskew is the timing uncertainty in the arrival of clock edges at FF1 and FF2 and T is the clock period [1].

(c) HOLD TIME

After the clock signal has changed, the input must be held for a period of time to allow the signal to propagate through the flip-flop for ensuring a stable output. This delay time is called hold time. The hold time may be negative, which means that the input signal may change before the clock changes and still ensuring the proper output value. As for other timing measurements, the hold time may differ for a low-to-high and high-to-low transition. Although state bit transitions must arrive by at least tsu seconds before the sampling clock edge, they also cannot arrive too early. This is because a flip-flop’s input must be held stable for a certain time th after the sampling clock edge. If state bit transitions travel very fast, they might arrive within th seconds of the clock edge and violate this requirement. To prevent this from happening, the delay of each combinational path between any two flip-flops must be large enough to satisfy the following condition:

tclk-q + tpd + tskew > th

where th is the hold time of the destination flip-flop.

The delay of a flip-flop can be expressed as the time taken from the input changes its state to the output has stabilized. The total delay can be expressed as tdelay = tsetup + tpcq, where tsetup is the time taken for the input to propagate and stabilize in the flip-flop, and tpcq is the time taken from the clock goes high to a valid output Q is available [1].

(d) CIRCUIT-LEVEL DESIGNS

Latches are the elementary blocks of computer memory. Every latch contains a positive feedback loop that has two stable electrical states corresponding to logic high and low. The loop is created by cross-coupling two inverting gates and typically contains an additional switch that opens or closes the loop. We can Design the flip-flops by using master slave latch. The latch is design by using transmission gate base logic NAND gates.

In metastability, the voltage levels of nodes A and B of the master latch are roughly midway between logic 1 (VDD) and 0 (GND). Exact voltage levels depend on transistor sizing (by design, as well as due to arbitrary process variations) and are not necessarily the same for the two nodes. However, for the sake of simplicity, assume that they are (VA = VB = VDD/2) [1].

(e) SYNCHRONIZATION

Connect the two instances in a series and use sequenced latching to allow them alternately. When one state register fails to latch the next state correctly, the latching sequence halt and the state is re-latched correctly in the next clock pulse. Flip flop synchronization is shown in fig 1. The both flip flops can be synchronize on
same clock.

**Fig 1:** Flip flop synchronizer

The synchronization failure in Dreg 1 may cause the failure in Dreg 2, but following cases may happen while the flip-flop synchronization.

**Fig 2:** Timing simulation of flip-flop synchronizer

**Case A**
At first clk pulse the Dreg 1 triggers and input D1 propagates at the output of Dreg1 which transfer to Dreg2 at second clk pulse.

**Case B**
The input D changes after setup and hold time will propagates at output of dreg1 at second clk pulse which arise at output of Dreg2 at third clk pulse.

**Case C**
The setup and hold time violation may cause failure in output of Dreg 1 which may recover before second clock pulse, cause the trigger of Dreg 2 at second clk pulse.

**Case D**
The setup and hold time violation may cause failure in output of Dreg 1 which may cause its output at low level and it synchronize input d at second and third clk pulse.

**Case E**
The setup and hold time violation may cause failure in output of Dreg 1 which may cause its output at high level and it synchronize input d at second and third clk pulse.

**IV. METHODOLOGY**

Synchronization failure can be reduce by using faster flip-flops. The latch snad flip-flops design using transmission gate which requires less number of transistors. Transmission Gate has the capability of a high-quality switch with small resistance and capacitance. Transmission gate is the part of our design module. The delay of the transmission gate can be modelled by linearized RC network. The on-resistance and diffusion capacitance of transmission gate is represented by a resistor.

\[ t_p = 0.69 \sum_{i=1}^{N} C_i \left( \sum_{j=1}^{i} R_j \right) \],
Transmission Gate is generally used to implement of XORs and MUXs with the minimum number of transistors. The flip-flops should be running on the same edge of your system clock as the rest of the circuit. This will limit the area of potential problems to one path instead of several, and minimize the possibility of metastability entering the main part of the circuit. Micro wind simulations were performed in order to quantify the delay, power and metastability performance of several flip-flops base modules. A CMOS layout is also implemented in MICROWIND Layout editor to represents the delay degradation due to metastability which affects the performance of circuits including timing simulation, power dissipation etc. The our work the flip-flop base module with both the master and slave stage protected with a excellent soft-error protection, significantly better than other flip-flops which only had protection on the slave stage. Moreover, we will show that flip-flop base module will have the best metastability performance. This indicates the differential feedback paths in the flip flop are a beneficial feature in improving metastability and offering soft-error protection. While the power and delay penalties are non-trivial, for robust application the flip-flop base module is attractive in terms of both soft-error protection and metastability performance. We will also try to improve the switching time of MOSFET device [4, 5].

V. CONCLUSION

It is impossible to completely prevent the synchronization failures but their probability can be reduced to an acceptable level by re-sampling the input signal through a cascade of flip-flops known as a synchronizer. This can be done by giving enough time for metastability to resolve to valid logic states before being interpreted by other circuits. Flip flop is a high gain circuit, it will amplify the input voltage and output becomes at stable state. Due to the setup and hold time violation the latch may have no initial voltage to amplify and thus the output of the flip-flop may become unpredictable and take an unbounded amount of time to settle to a stable level. Due to the setup and hold time violation the latch may have no initial voltage to amplify and thus the output of the flip-flop may become unpredictable and take an unbounded amount of time to settle to a stable level.

Reference:


