

# Design of Low Power One-Bit Hybrid-CMOS Full Adder Cells

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**Abstract**—The aim of our work is to evaluate the performance of One-bit Hybrid full adder cell. To achieve a good-drivability, noise-robustness, and low energy operations for deep-sub micrometer, we explore Hybrid-CMOS style design. Hybrid-CMOS design styles utilize various CMOS logic style circuit to build new Full Adder with desired performance. This Full Adder is categorized into three modules. We compared the proposed Full Adder cell with conventional static CMOS logic styles Adder Cells like C-CMOS, CPL, TFA, TGA and with some hybrid cells at different Load condition. Each Cell showed different power consumption, Delay, PDP and driving capability. The circuits being studied are optimized for energy efficiency at 0.18 $\mu$ m CMOS process Technology.

**Keywords**—Full Adders, Hybrid CMOS Design style, deep-sub micrometer technology, low power, Delay & PDP.

## I. INTRODUCTION

The tremendous growth in portable electronics systems, the designers prime research are in low power nanoelectronics technology to achieve a good-drivability, noise-robustness and low-energy operations for deep-sub micrometer and to extend the battery life of the system.

Full adders are fundamental cell in various circuits which is used for performing arithmetic operations such as addition, subtraction, multiplication, address calculation and MAC etc. Enhancing the performance of the full adders can significantly affect the whole system performance.

Hybrid CMOS logic styles have a higher degree of design freedom to target a desired performance. A 1-bit Hybrid Full Adder cell which has higher speed, less power consumption and higher performance and reliability by scaling supply voltages toward deep-sub micrometer technology.

Reduction of the threshold voltage in deep-sub micrometer technology and scale down the supply voltages are the most effective way to reduce power consumption. However sub-threshold leakage current increases exponentially when threshold voltages are reduced. At low threshold voltage, leakage power becomes a issue. At deep-sub micrometer technology, the benefits of lower V<sub>dd</sub> will be of no use more because of problems of leakage power. Due to lowering V<sub>dd</sub>,

it causes increase in circuit delay and decreases PDP & degrades the drivability of cells designed with certain logic styles. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may increases the propagation delay of a circuit [2]. Reducing the number of and magnitude of the circuit capacitances, and reducing the spurious transitions in the output signals are some of the techniques used at the circuit level to reduced the power consumption [3].

Many previously adders are suffered from the problem of low swing and high noise when operated at low supply voltages. The proposed full adder circuit have operated successfully at low V<sub>dd</sub>'s with good driving capability and noise robustness.

The remainder of the paper is organised as follows. Section II gives a brief survey of previous work in which logic styles are compared. Section III consists of explanation of proposed work. Section IV includes analytical comparisons and results and Section V gives a conclusion.

## II. PREVIOUS WORK

Several logic styles have been used in the past to design full adder cells. Each design styles have its own merits and demerits [2].

A classical design of standard static CMOS full adder is based on regular CMOS structure with conventional pull-up and pull-down transistor providing full-swing output and good driving capabilities. The existence of the PMOS block in static CMOS circuits is a main drawback because it has low mobility compared to the NMOS. Hence, there is a need to be sized up to get desired performance.

A complementary Pass Transistor Logic (CPL) is another conventional adder [2], which provides high speed, full-swing operation, and good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors. But due to the presence of a lot of internal nodes and static inverters, there is large power dissipation.

TFA and TGA are based on transmission function theory and transmission gates respectively. These are inherently low power consuming. The main drawback is that they lack

driving capability. All of the published work shows that the TFA outperforms the conventional CMOS Adder from the power consumption point of view [4].

The other Full adders using Hybrid CMOS logic styles are new 14T [6] and hybrid pass logic with static CMOS output drive full Adder HPSC [7] in an attempt to build a low power full adder cell.

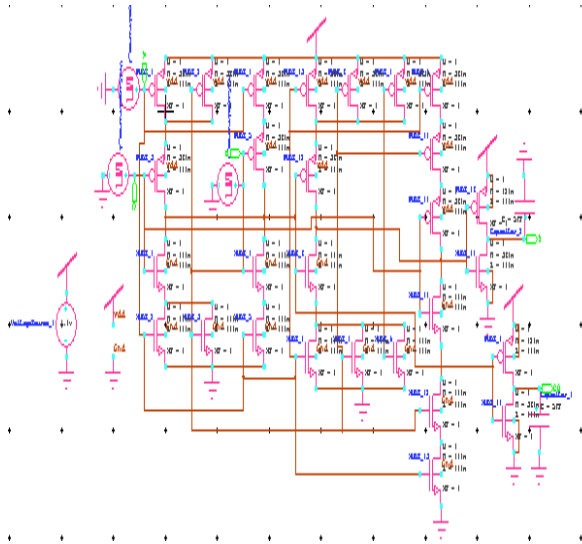


Figure (a): C-CMOS

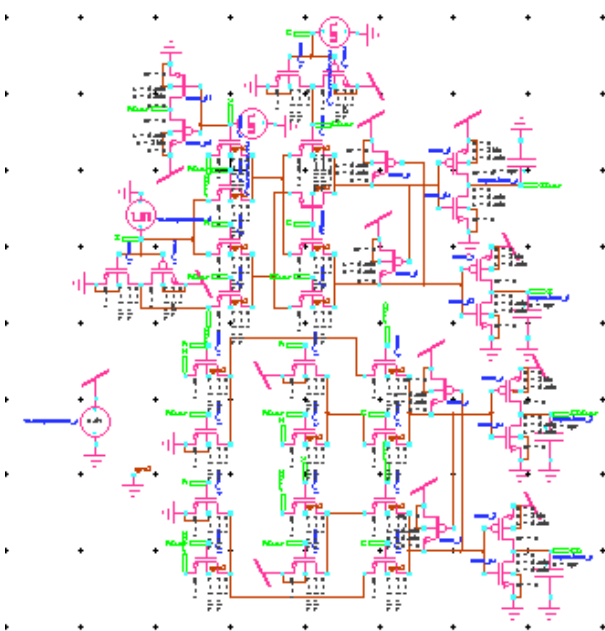


Figure (b): CPL

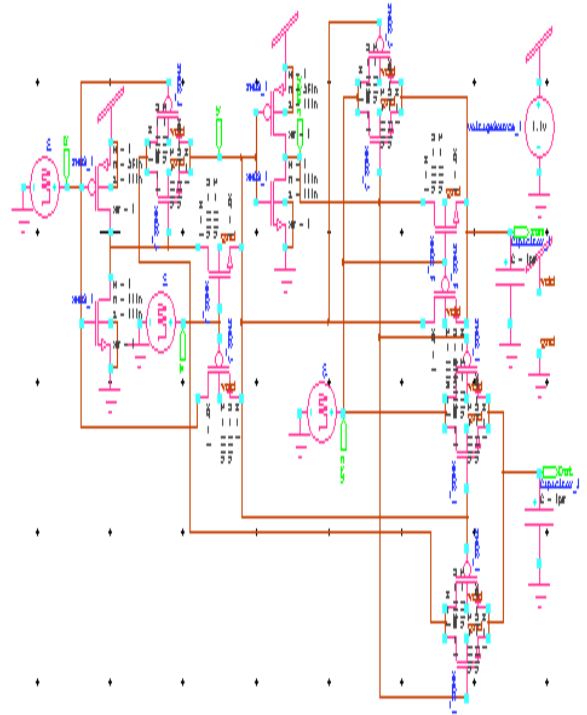


Figure (c): TFA

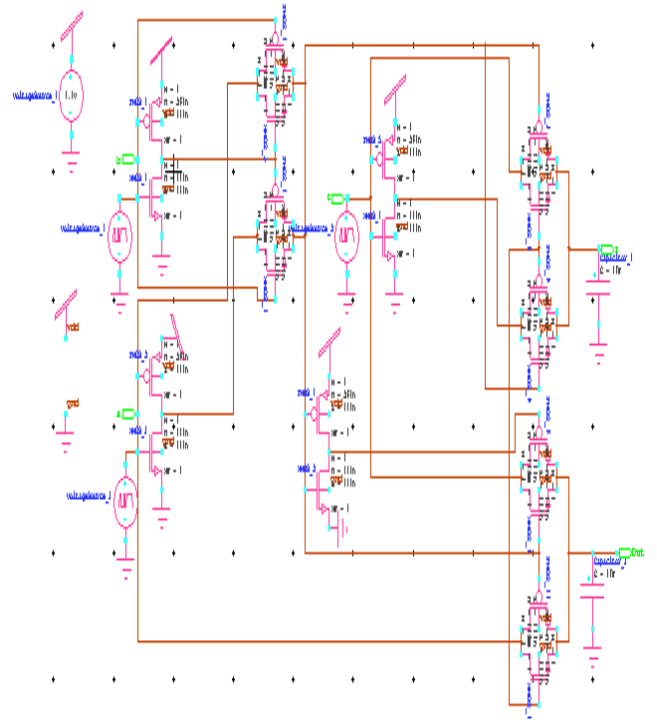


Figure (d): TGA

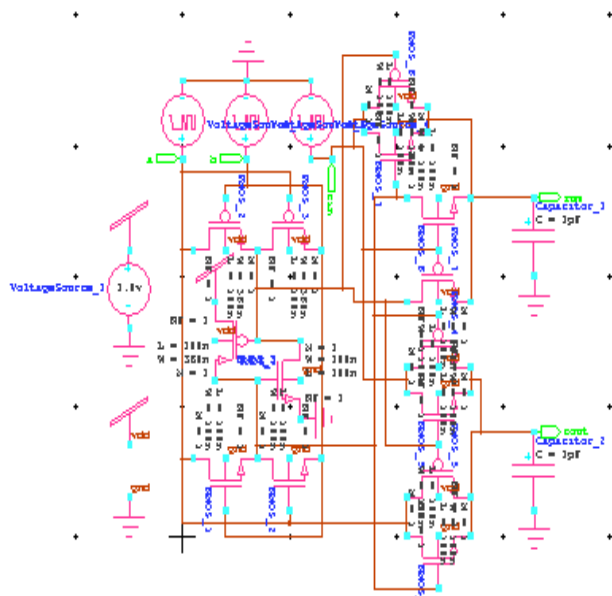


Figure (e): New 14T

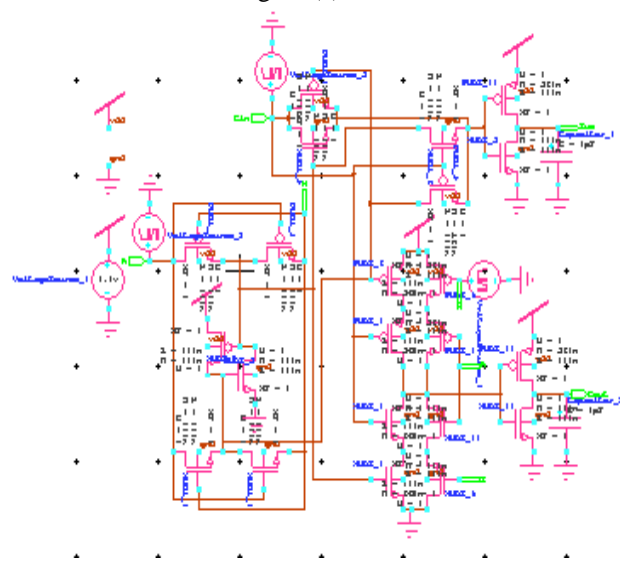


Figure (f): HPSC

The Boolean expression for Sum and Cout for one-bit Full adder circuit is as follows.

$$S = A \text{ xor } B \text{ xor } C_{in}$$

$$S = H \text{ xor } C_{in} \text{ Where } H = A \text{ xor } B$$

$$C_{out} = A.H' + C_{in}.H$$

This provides a full-swing operation and can operate at low voltages also. A hybrid-CMOS full adder can be broken down into three modules. Module I comprises of either a XOR or XNOR circuit or both. This module produces intermediate signals that are passed onto Module II and Module III that generate Sum and Cout outputs, respectively.

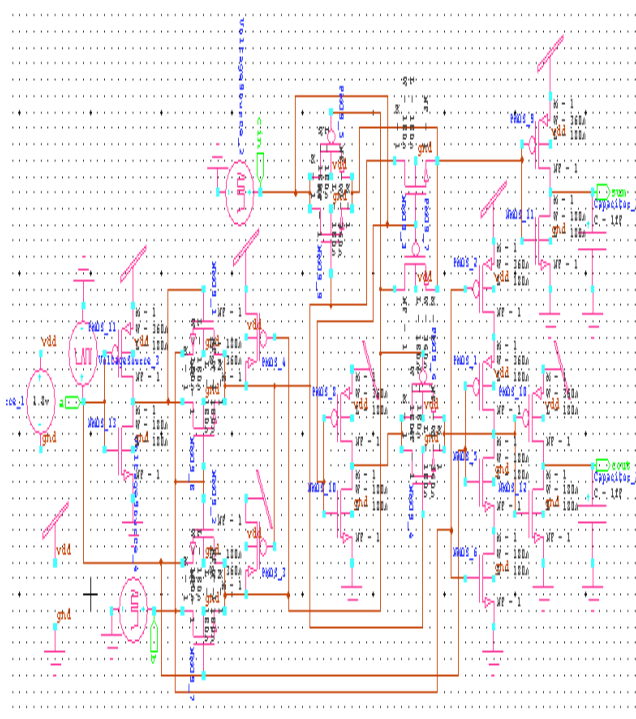
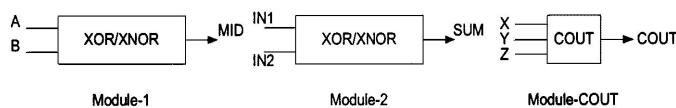


Figure (f): Hybrid-CMOS FA

There are three major components of power dissipation in CMOS Circuits [5].

- a) Switching power: power consumed by circuit node capacitance during transistor switching.
- b) Short-circuit power: power consumed due to current flowing from Vdd to Gnd when both transistors are ON.
- c) Static power: Due to Leakage and static currents.

### III. PROPOSED WORK

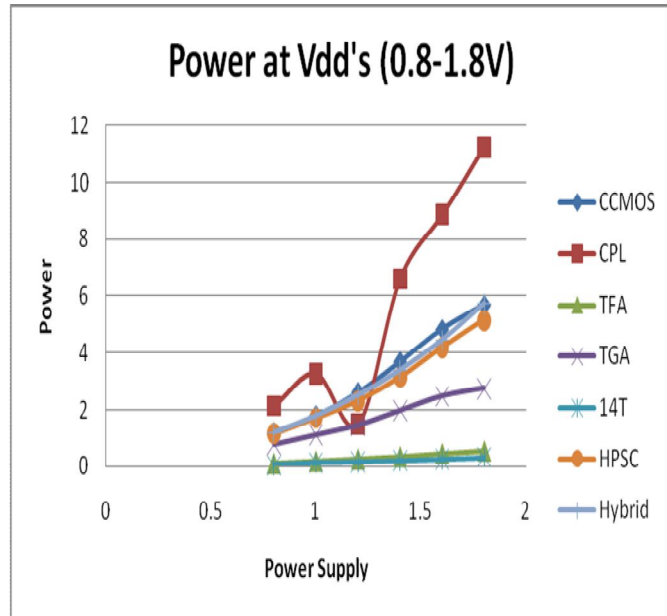
### IV. RESULT AND ANALYSIS

We calculated Power consumption at different power supplies ranges (0.8-1.8V) for all mentioned full adder circuits. Also we calculated delay between Cin & Cout . The circuits were simulated in T-spice at different Vdd's, at 50Mhz,25degree celcius.

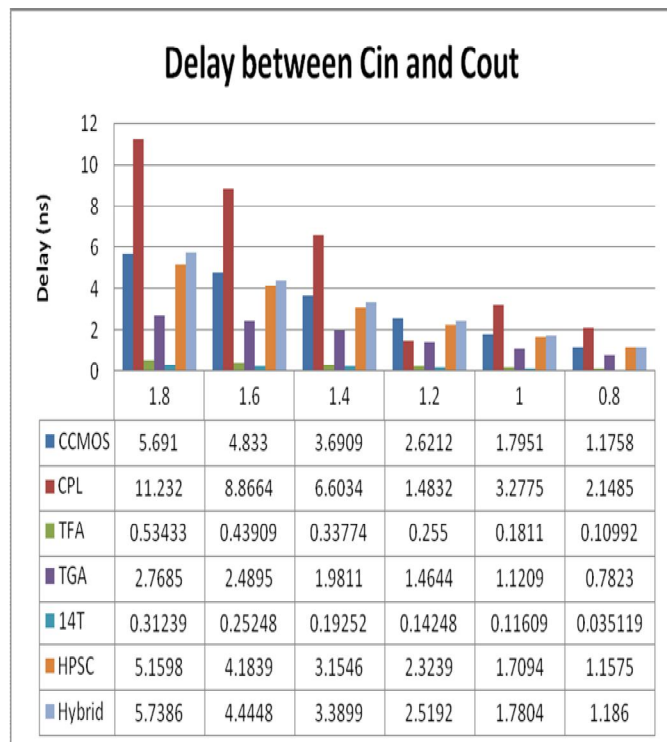
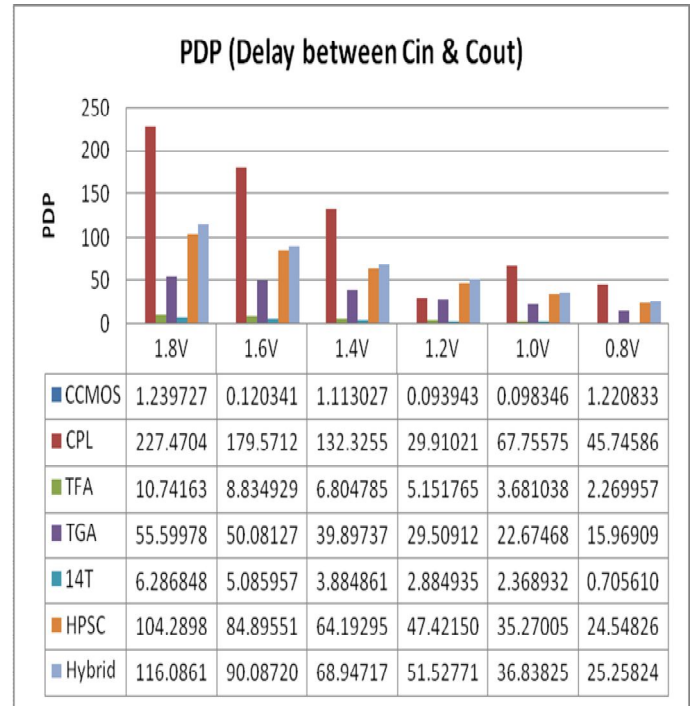
By optimizing the transistor sizes of the full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. All

adders were designed with minimum transistor sizes initially and then simulated.

To achieve minimum PDP, an iterative process of redesigning and transistor sizing after post-layout simulations was carried out.



Among conventional adders, the adders without driving capability (TGA and TFA) have the lowest PDP. The PDP of TFA is lesser than that of TGA for higher voltages but the trend reverses for lower voltages suggesting that from energy point of view TGA is a better choice. Among adders with driving capability, the CPL adder as expected has the highest PDP amongst the conventional adders.



Despite having lowest PDPs, TGA and TFA performances degrade drastically with increasing output loads. This shows that although these adders show good performance as standalone units, if cascaded or used in a high fan-out situation, they may not deliver the required performance. This is because the input is not decoupled from the output. In a real circuit, buffers have to be inserted in between two adders to assure good signal strength. This will increase the delay as well as the power consumption of the whole design.

In the case of nonconventional or hybrid-CMOS adders, the proposed hybrid-CMOS full adder displays the best PDP characteristics for both varying supply voltages and output loads.

Inverters at the output of module II and module III ensure sufficient drive strength. Moreover, the power dissipation result of the proposed full adder includes the power consumed by the two output inverters, and still is less than other conventional designs. The performance of the new full-adder cell is attributed to the proposed XOR–XNOR circuit and the novel hybrid-CMOS output module. As shown earlier, these

circuits show good improvement in PDP and are faster compared to their counterparts.

The remaining two hybrid-CMOS adders (HPSC and NEW14T) have poor PDP characteristics. For low supply voltages, the PDP rises drastically making them unsuitable for low-voltage operation.

## V. CONCLUSION

Hybrid-CMOS design style gives more freedom to the designer to select different modules in a circuit depending upon the application. Using the adder categorization and hybrid-CMOS design style, many full adders can be conceived.

This full adder designed using hybrid-CMOS design style is used to target low PDP.

The hybrid-CMOS full adder has better performance than most of the standard full-adder cell. It performs well with supply voltage scaling (1.8V – 0.8V) and under 0.02pF Load conditions.

This Full adder has better noise immunity as compared to the standard adder such as static CMOS, making it suitable for deep-sub micrometer operation. We recommend the use of hybrid-CMOS design style for the design of high-performance circuits.

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