Voltage Balancing Control of Neutral-Point Clamped Inverters Using Multi Carrier Pulse Width Modulation for FACTS Applications

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Abstract— In this paper, a novel technique used to keep the voltage across the dc split capacitors of neutral point clamped inverter using multi carrier pulse width modulation and also compensate the reactive power. It can reduce the harmonics without any changes in inverter output. Multi carrier pulse width modulation is controlling the neutral point voltage at full modulation index. It require compensation loop because it does not deliver the natural voltage balancing. The voltage is balanced under all operating conditions. The main task of controller is to force the current vector in the three phase load. The effectiveness of the proposed method is verified by simulations and experiments.

Keywords— FACTS, GTO, multilevel, multi carrier PWM, NPC inverter, voltage balance.

I. INTRODUCTION

Numerous industrial applications have begun to require high power apparatus in the recent years. Some motor drives and utility applications require medium voltage and megawatt power [3][12][15]. For a medium voltage grid, it is bothersome to connect only one power switch directly. A structure of multi-level inverter is introduced as high power and medium voltage. A multilevel inverter not only accomplishes high power applications and also enable for renewable energy sources such as wind, solar and biomass energy. However, a multilevel inverter to reach high power is to use a series of power semiconductor switches with several dc sources to implement the power conversion by staircase waveform. Capacitors, batteries and renewable energy voltage sources can be recycled s multiple d sources.

A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The main topology of multilevel inverters is diode clamped inverter, flying capacitor and cascaded H-bridge inverter. Neutral Point Clamped Inverter is more preferred than other topology. Nowadays Neutral point clamped inverter have important development to achieve high power with dissimilar voltage level and also deliver more advantages than conventional inverter. Such as, low switching losses, high power quality of waveform without certain order harmonics and reduced output dv/dt. But these features are obtained when the voltage across the capacitor is balanced under different working conditions.

Fig.1: main power characteristics for the MV100-INGECON WIND converter system.

The main problem of Neutral Point Clamped inverter is balance the voltage across the dc split capacitors. Several modulation strategies have been developed for multilevel inverter. The most common used is multicarrier pulse width modulation (PWM). The multi carrier pulse width modulation
is classified into two types. There are multi carrier sub harmonic pulse width modulations and multi carrier switching frequency optimal pulse width modulation. The multi carrier sub harmonic pulse width modulation scheme reduced total harmonic distortion at high switching frequency. In this paper multi carrier pulse width modulation scheme is preserved. To improve the harmonic characteristics of three phase multi-level inverter have been discussed.

II. NEUTRAL POINT CLAMPED INVERTER

Neutral point clamped inverter proposed by Nabae, Takahashi. In 1990’s several researchers published articles that stated experimental results for four-, five-, six-level Neutral point clamped inverters for such uses as high power application and FACTS devices[22][25][18][19].

In this paper twenty one level Neutral point clamped inverter is discussed. A Common dc bus provides the dc source to each three phase of Neutral point clamped inverter. A common dc bus has been subdivided by fourteen capacitors into twenty one levels. The voltage across each capacitor is Vdc and voltage stress across each switching device limited into dc source through the clamping diodes. Switch is ON when the state condition is 1 and the switch is OFF when the state condition is 0.

Each phase has fourteen switch pairs such that turning ON one of the switch pair requires that other pair is turned OFF. The switch pair for phase leg a (Sa1, Sa’1), (Sa2, Sa’2), (Sa3, Sa’3), (Sa4, Sa’4), (Sa5, Sa’5), (Sa6, Sa’6), (Sa7, Sa’7), (Sa8, Sa’8), (Sa9, Sa’9), (Sa10, Sa’10), (Sa11, Sa’11), (Sa12, Sa’12), (Sa13, Sa’13), (Sa14, Sa’14), (Sa15, Sa’15), (Sa16, Sa’16), (Sa17, Sa’17), (Sa18, Sa’18), (Sa19, Sa’19), (Sa20, Sa’20) and (Sa21, Sa’21).

For a twenty one level inverter, a set of fourteen switches is on at given time. The line voltages are Vab, Vbc, and Vac. The line voltage VAB is consists of leg a and leg b, the resulting line voltage is twenty nine level staircase waveform. This means an m-level inverter is deliver the output phase voltage is m-level and an m-level inverter is deliver the output line voltage is K=2m-1 level. The number of clamping diodes are Dc=2m-1.

Each active switching is required to voltage level of Vdc and each clamping diodes require different rating for reverse voltage blocking. Using phase a when all the lower switches S’a1 to S’a14 turned on, D4 must block 4Vdc. Similarly D3, D2, D1 must blocks 3Vdc, 2Vdc, 1Vdc respectively. If each blocking voltage has same voltage as active switches, Dn will require n diodes in series. The number of diodes required for each phase would be (m-1) (m-2). Thus, the number of blocking diodes is quadratically related to the number of levels in a neutral clamped inverter.

One application of neutral point clamped inverter is voltage speed drives for high power. Another application is an interface between a high voltage DC transmission line and an AC transmission line. Main advantage of neutral point clamped inverter is efficiency is high and all phase shares common dc bus which minimizes capacitance requirement. Disadvantage is requirement of clamped diode is high.

III. MULTI CARRIER PULSE WIDTH MODULATION

Several different two-level multilevel carrier-based PWM techniques have been extended for controlling the active devices in a multilevel converter. The easiest technique to implement uses several triangular carrier signals and one reference. Sub harmonic pulse width modulation and switching frequency optimal pulse width modulation are very popular method in industrial applications.

The principle of multi carrier pulse width modulation (MC-PWM) is based on a comparison sinusoidal reference waveform with triangular carrier waveform. To generate m level it required m-1 carrier. Amplitude Ac and frequency Fc of both carrier and reference waveform are same. A frequency of sine reference waveform is Fr and peak to peak value of reference waveform is Ar. If the triangular carrier is greater than reference signal the result is 1 otherwise 0. Sum of the different comparison which represents voltage level is output modulator. The scheme is characterized by amplitude modulation index m1 and frequency modulation index m2.

Having more than two levels to build sinusoidal shape it is instinctual that it can reduce the harmonics in load. However, the improvement of current is depends on the controller employed. The sub harmonic pulse width modulation is more popular because of its simplicity and a good result for all the operating condition includes over modulation. In the case of three phase inverter three legs are produced. Requirements of three phase system 120° phase shifted modulation sinusoids are needed. Two possibilities are renowned by use of carrier signal.

The carriers have the same frequency and same amplitude and are disposed so that the bands are continuous.

Fig. 2. A typical output waveform
First, single carrier used to compare with three modulation sinusoid. Second, three different carrier sets with 120° phase displacement compared with corresponding sinusoid. In the middle of the carrier set zero reference is placed. Each carrier is compared with modulating signal at every instant.

For a sine waveform (reference) cantered in the carrier bands, the duration of time that the waveform exists.

For an \( m \)-level inverter, \( m-1 \) carriers with the same frequency \( f_c \) and the same amplitude \( A_c \) are disposed such that the bands they occupy are contiguous. The reference waveform has peak-to-peak amplitude \( A_m \), a frequency \( f_m \), and its zero centred in the idle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active devices corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active devices corresponding to that carrier is switched off.

In multilevel inverters, the amplitude modulation index, \( m_a \), and the frequency ratio, \( m_f \), are defined as

\[
M_a = \frac{A_m}{(m-1) A_c} \\
M_f = \frac{f_c}{f_m}
\]

Where,  
\( m \)- The number of carrier waves. 
\( A_m \) and \( f_m \) are the amplitude and frequency of the reference wave.  
\( A_c \) and \( f_c \) are the amplitude and frequency of the carrier wave.

Another carrier based method that was extended to multilevel applications is termed switching frequency optimal PWM, and it is similar to SH_PWM except that a zero sequence voltage is added to each of the carrier waveforms. This method takes the instantaneous average of the maximum and minimum of the voltages \( (V_a^*, V_b^*, V_c^*) \) and subtracts this value from each of the individual reference voltages i.e.

\[
V_{offset} = \max (V_a^*, V_b^*, V_c^*) + \min ((V_a^*, V_b^*, V_c^*))
\]

\[
V_{aSFO} = V_a^* - V_{offset}
\]

\[
V_{bSFO} = V_b^* - V_{offset}
\]

\[
V_{cSFO} = V_c^* - V_{offset}
\]

The SFO-PWM technique enables the modulation index to be increased by 15 percent before the over modulation region is reached.
IV. HYSTERESIS CONTROLLER

To determine the switching signals and control the supply current for inverter gates, the hysteresis band is used. When the supply current exceeds the upper band, the comparators generate control signals in such a way to decrease the supply current.

The implementation of hysteresis controller is very simple and robust and it provides a quick and easy response in the system. By comparing the error signal with that of the hysteresis band it generating the required triggering pulses and it is used for controlling the voltage source inverter that the output current is generated from the filter will follow the reference current waveform is shown in figure.

Fig. 7. Hysteresis Control

It controls the switches of the voltage source inverter and to ramp the current, so that it follows the reference current. The ramping of the current between the two limits where the upper hysteresis limit is the sum of the reference current and the maximum error or subtraction of the reference current and maximum error is shows in the figure.

If the value for the minimum and maximum error should be the same, the hysteresis bandwidth is equal to two times of error. When the error reaches an upper limit, the transistors are switched to force the current down. When the error reaches a lower limit the current is forced to increase. The range of the error signal directly controls the amount of ripple in the output current from the inverter.

The hysteresis limits, \( e_{\text{min}} \) and \( e_{\text{max}} \), relate directly to an offset from the reference signal and are referred to as the Lower Hysteresis Limit and the Upper Hysteresis Limit. The current is forced to stay within these limits even while the reference current is changing.

V. ANALYSIS OF FIFTEEN LEVEL NEUTRAL POINT CLAMPED INVERTER

A three phase fifteen level neutral point clamped inverter is shown in the fig. each phase is constituted by 28 switches. The Switches \( S_{a1} \) through \( S_{a14} \) of upper leg form balancing pair with the switches \( S'_{a1} \) through \( S'_{a14} \) lower leg of the same phase. For example a nine level inverter is shown in the figure.

Fig. 9 A typical Multilevel Inverter

By comparing the reference waveform the output voltage is produced. The input voltage and currents are

\[
\begin{align*}
    i_A &= \bar{I} \sin (\omega t + \phi) \\
    i_B &= \bar{I} \sin \left(\omega t - \frac{2\pi}{3} + \phi\right) \\
    i_C &= \bar{I} \sin \left(\omega t + \frac{2\pi}{3} + \phi\right) \\
    v_A &= E/2 m_1 \sin (\omega t) \\
    v_B &= E/2 m_{11} \sin \left(\omega t - \frac{2\pi}{3}\right) \\
    v_C &= E/2 m_{1} \sin \left(\omega t + \frac{2\pi}{3}\right)
\end{align*}
\]

If the phase voltages and currents to be zero sequence but not the negative sequence, the average current entering the
midpoint of the dc-bus provided by phase A must be same as that provided by phase B and phase C. If all the harmonics are in sine phase, this is all cross the zero level, at the same angle with positive slope. When the derivative gets close to zero at the opposite angle, the limit for that condition is met.

An algebraic expression for the linearity condition is obtained as follows:

\[ V = \sum_{h} m_h \cdot \sin(h \cdot \omega t) \]
\[ \frac{dV}{dt} = \sum_{h} h \cdot m_h \cdot \cos(h \cdot \omega t) \]
\[ \left. \frac{dV}{dt} \right|_{\omega = \text{odd}} = \sum_{h \text{ even}} h \cdot m_h \cdot \text{even} - \sum_{h \text{ odd}} h \cdot m_h < 0. \]

For small enough amplitudes of the injected harmonics, the gains obtained with this method. For second harmonic compensation:

\[ v_A = \frac{E}{\pi} m_1 \cdot \sin(\omega t) + \frac{E}{\pi} m_2 \cdot \sin(2 \cdot \omega t) \]
\[ i_M = 3 \cdot i_{m-A} = -\frac{6 \cdot I}{E} \int_0^\pi v_A \cdot \cos(\omega t) \cdot dt \]
\[ = -\frac{6 \cdot I}{E} \int_0^\pi \frac{E}{2} m_2 \cdot \sin(2 \cdot \omega t) \cdot \cos(\omega t) \cdot dt \]
\[ = -\frac{3 \cdot I}{\pi} \int_0^\pi \sin(2 \cdot \omega t) \cdot \cos(\omega t) \cdot dt \]
\[ i_M = \frac{4 \cdot I}{\pi} \int_0^\pi \sin(2 \cdot \omega t) \cdot \cos(\omega t) \cdot dt \]

Already we well have known that second harmonic currents are restricted in power quality standards. However, it’s expected to be small and negligible at the output. And it is usually injected during the short transient periods.

**V1 CONTROL STRATEGY**

To achieve good voltage balancing performance must be applied proper offset. The offset is added with the opposite sign to the modulation signals of each phase. If the offset value is low, a slow voltage-balancing dynamic on the dc-split capacitors is produced. If the value of the offset is high the system dynamic is slow. The voltage balancing control variable is the neutral point current \( i_0 \) \[6]\[18] \ . In the steady state condition the average value of this variable is zero.

The current injected into the neutral point inverter which the output phases are connected to that point and the output currents are \( i_a, i_b, i_c \) by the following expression are described the currents \( i_a \) and \( i_c \):

\[ \bar{I}_a = \bar{i}_{cm} + i_{a2} \]
\[ \bar{I}_c = \bar{i}_{cm} + i_{c2} \]

\[ \bar{I}_{a2} = i_{cm} + i_{a2} / 2 = c \cdot v_{dc} / 2 - v_{c2} / T_3 \]
\[ \bar{I}_{c1} = i_{cm} + i_{c2} / 2 = c \cdot v_{dc} / 2 - v_{c1} / T_3 \]

The locally averaged currents should be

\[ \text{Fig. 10. Current in the capacitors.} \]

For the modulation signals in phase \( a \) is given as follows. The duty cycle for the connection of this phase to the neutral point is obtained. An example calculation of the offset is needed.

\[ d_a = -d_b i_b(k+1) - d_c i_c(k+1) \]

By adding an offset to the modulation signals, the duty cycle \( d_a \) is changed. The NP current can be calculated as follows:

\[ \bar{I}_a(k+1) = d_a i_a(k+1) + d_b i_b(k+1) + d_c i_c(k+1) \]

Now \( i_a(k+1) \) is different from zero. And the new duty cycle is

\[ d_a'(k+1) = \frac{\bar{I}_a(k+1) - d_b i_b(k+1) - d_c i_c(k+1)}{i_a(k+1)} \]

Where

\[ d_a' = \sqrt{|v_{an}^* - v_{aj}^*|} + 1 \]
\[ \frac{d'v}{dv} = \frac{-d\theta_v (k+1)}{d\theta_v (k+1) - d\theta_i(k+1)} + 1 \]

The relationship between the above equations is

\[ d'v / dv = \left\{ \begin{array}{lc} \bar{i}_o(k+1) & -d\theta_v (k+1) - d\theta_i(k+1) \\ \end{array} \right\} + 1 \]

### TABLE 1

**POSSIBLE CASES FOR SIMPLIFICATION**

\[ V_{an} = V_{an} - V_{ap} + I \]

All duty cycles must be positive. Sign and relative magnitude of the variables are taken into account in the eight possible cases it shows in table 1. The sign variables are (+) and (-). For simplicity we used the variables \( x \) and \( y \).

Where,

\[ x = V_{an} - V_{ap} + I \]

\[ y = 2V_{a-off} \]

The relationship between the modulation signals and the compensation is determined by taking into account the value of the duty cycle. Its shows in the following expression:

\[ d'v / dv = \left\{ \begin{array}{l} \bar{i}_o(k+1) \\ \end{array} \right\} + 1 \]

\[ d'v = \left\{ \begin{array}{l} \bar{i}_o(k+1) \\ \end{array} \right\} + 1 \]

### TABLE II

**POSSIBLE CASES PER PHASE**

The mathematical process for the other phases is the same as the phase a. Table II shows the offset for the three phases. The equations define the optimal offset value they include the relevant variables and the system dynamics, the modulation index, the carrier frequency, the dc split capacitor values, and the corresponding capacitor voltages.

### VLSIMULATION RESULT

For a modulation index 0.8 a twenty one level inverter is simulated. The inverter was supplied by an ideal current source and phase to phase voltage was 100v. The reference frequency is 48.9Hz and the carrier frequency is 2440Hz.

The total harmonic distortion is 4.28%. For 100Hz, the total harmonic distortion is 3.27% and for 150Hz, the total harmonic distortion is 1.82%. It’s shown in the figure 4. By the inverter has sharp edges, the voltage waveform is produced. Simulation result of the proposed scheme reduced voltage and current THD.
Fig. 11. The simulation result of FFT Analysis

For 250Hz, the total harmonic distortion is 1.01% and for 300Hz, the total harmonic distortion is 0.63%. Its shows in figure 5.

Fig. 12. FFT Analysis

When a triangular carrier wave has its peak coincides with zero of the reference wave there are number of pulses per half cycle is

\[ P = \frac{m_f}{2} \]

There is (p-1) number of pulses per half cycle when zero of the triangular carrier wave coincides with zero of the reference wave.

The harmonics pushes by PWM into a high frequency range around the switching frequency. The frequencies at which the voltage harmonics occur can be described by

\[ f_n = (j.m_f \pm k) \cdot f_s \]

The \( n \)th harmonic is calculated by

\[ n = j \cdot m_f \pm k = 2jp \pm k \]

For modulation index less than 1, largest amplitudes in the output voltage are associated with harmonics. It increasing the number of pulses per half cycle and also the harmonic frequency can be raised which can be filtered out easily.

Compared other inverters the NPC inverter is provide high quality output without certain order harmonics. By using multicarrier PWM the total harmonic distortion is reduced. Its shows in the simulation result. And also compensate the reactive power. The efficiency is high and it’s a transformer less strategy. So the size of the circuit reduced and using small size of filter. This method is used in FACTS applications and renewable energy applications. But the disadvantage of this topology is the installation cost is high and the source is not isolated.

Fig. 13. simulation result for Output current

Fig. 14. simulation result for 3 phase output voltage
VIII. CONCLUSION

This paper has presented a novel technique to balance the voltage of the dc split capacitors of 21-L neutral point clamped inverter, suitable for reactive power compensation and also reduce the harmonics, when multi carrier PWM modulation is employed. It consists of more carrier waveform and one reference waveform. The switching frequency of multi carrier PWM can be less than or greater than the carrier frequency and the function of displacement phase angle between carrier set and modulation waveform. In the multi-level PWM switching strategies, switching losses can be minimized by adjusting the displacement phase angle for a more efficient multilevel inverter. A novel carrier-based switching strategy can be used to enable better switch utilization. The contribution of current to the inverter midpoint has been analyzed.

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