DC-DC Converters Using PID Controller and Pulse Width Modulation Technique

R.Sudha¹ Mr.P.M Dhanasekaran² ¹PG Scholar ²Assistant Professor Department of Electrical and Electronics Engineering, K.S.Rangasamy College of Technology, Tiruchengode, Tamilnadu, India

Abstract- This paper presents a boost converter along with a flyback converter. The Zero Voltage Switching (ZVS) technique is used to achieve soft switching. A bidirectional boost converter is connected with an output module as a Parallel Input Serial Output configuration. The flyback converter with Voltage Doubler Rectifier (VDR) acts as an output module. This connection makes a bidirectional boost converter an active clamp circuit which is connected to the output side in order to extend the step up ratio. A converter with active clamp technique is used to recycle the leakage energy, to eliminate voltage spike due to coupled inductors and also to provide a mechanism to achieve ZVS. To overcome the efficiency degradation during light load due to load dependent soft switching of the ZVS, a control method using Pulse Width Modulation (PWM) proportional to the load current is used.

Key words: Zero Voltage Switching (ZVS), Voltage Doubler Rectifier (VDR), step up ratio, Pulse Width Modulation (PWM)

I. INTRODUCTION

Many applications such as electric vehicles (EV), photovoltaic (PV) grid connected power systems, high intensity discharge (HID) lamp ballast used in automotive headlamps in which the start up voltage is up to 400 V, the DC-DC converter needs to boost the 12 V of the battery voltage up to required level. Generally speaking, the high step-up DC-DC converters for these applications have the following common features.

- 1) High step-up voltage gain
- 2) High efficiency
- 3) No isolation is required

However the step up capability is limited due to parasitic resistances, the reverse recovery problem caused by a high voltage rating of the diode and the large switching losses due to the hard switching. These are the major obstacles not allowing the high step-up ratio and efficiency.

To handle these concerns, several converter topologies adopting the voltage conversion ability were adopted which had several drawbacks. The usage of voltage multiplier cells [2]-[4], increases the step up ratio by including one multiplier capacitor and diode for each phase. Hence, as the output voltage is increased the number of stages also gets increased demanding more number of capacitors and diodes. As the number of capacitors and diodes are increased, the losses and cost also get increased and the circuit designing becomes more complex. A coupled-inductor is employed as a favorable step-up technique because of its simple structure [5]-[7]. By using coupled inductor the voltage and current stresses of the active switches can be reduced. It can achieve a high efficiency and protect the switch from the high peak voltage. But the voltage stress on the boost diode is increased and high voltage operation of the diode might induce a high reverse recovery problem. Besides, as the auxiliary turns of the coupled inductor are increased to raise a step-up ratio further, an input current ripple becomes larger in return. Thus, more input filter is needed.

Another easy approach for a high step-up ratio is the current fed type converters using a transformer [8]-[11]. A transformer leakage inductance causes a voltage spike across the switches so that a snubber circuit is required, resulting in additional loss. The active clamp approach similar to that applied on the coupled-inductor scheme releases these problems and reduces switching losses by using its soft switching capability. Unfortunately, the clamp capacitors are connected on the input side so that it has no function of extending a step up ratio.

Focused on the step-up ratio extension with the concept of the stacked output capacitors, the high step-up boost-sepic converter is proposed in [13] and flyback converter is proposed in [16], [18], and [19] and improved with a secondary voltage-doubler rectifier. Despite their high step-up capability, the switch suffers from the hard switching losses.

As a desirable solution to the above mentioned drawbacks, this paper proposes DC-DC converters using active clamp technique and pulse width modulation control. It integrates a bidirectional boost converter with a series output module as a Parallel Input Series Output (PISO) configuration. This connection makes the bidirectional boost converter as a active clamp circuit. Therefore it uses the step up capability of the stacked output capacitors while maintaining the soft switching capability of the active clamp circuit.

However the proposed converter has a load-dependent ZVS condition, which is an inherent characteristic of the activeclamp circuit. It causes hard switching at a light load and degrades conversion efficiency. To recover ZVS at a light load, a control method using Pulse Width Modulation (PWM) is also proposed.

II. BLOCK DIAGRAM

The block diagram of the proposed system is shown in fig 1. It consists of flyback converter and boost converter. The boost converter used is bidirectional boost converter.

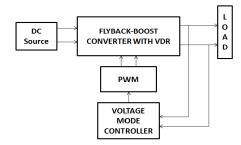


Fig 1. Block Diagram

The soft switching is achieved by using zero voltage switching in order to reduce the switching losses. The bidirectional boost converter act as an active clamp circuit. VDR is adopted at the secondary side to clamp the output rectifier voltage stress. Also this VDR contributes the increase in a step-up ratio further. Thus the proposed converter has the high step-up capability with the help of ZVS Bidirectional Boost Converter with flyback converter and VDR. With the features of ZVS, the proposed converter can ensure the high operating frequency, high step-up ratio, low voltage stresses across the switches and output rectifiers, soft switching of all switches, and so on.

The voltage mode controller utilizing the PID control law is executed for regulating the output voltage cycle by cycle, since the sampling pulse is updated with the updated pulse. To improve the efficiency degradation during light load condition, PWM control is used. According to the load, the pulse width modulator generates pulses according to which the converter is turned ON or OFF and regulates the output.

III. CIRCUIT DIAGRAM

The circuit diagram of the boost converter and a flyback converter along with a voltage doubler rectifier is shown in fig 2.

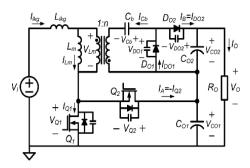


Fig 2. Circuit diagram of ZVS flyback-boost converter with VDR

A VDR is adopted at the secondary side to clamp the output rectifier voltage stress. To increase the device utilization and simplify the circuit, the common parts integration between the bidirectional boost converter and flyback converter is recommended. As shown in Fig.2, a bidirectional boost converter and a flyback converter can be integrated easily since the inductor L_A and switch Q_1 become common parts for both bidirectional boost converter and flyback converter.

III (a) High Step-Up Capability

Due to the stacked output capacitors, each output capacitor voltage is added and the overall output voltage can be extended as

$$V_0 = V_{C01} + V_{C02}$$
 (1)

That is, the output voltage of the converters is a sum of the output voltages of the boost converter and the flyback converter, which is suitable for high step-up applications.

III (b) Switch Voltage Stress Clamping

The switch voltage stresses V_{Q1} and V_{Q2} can be clamped to the partial output voltage V_{CO1} . Thus ,additional protection circuit for the high voltage spike caused by a leakage inductor L_{lkg} is not required.

III (c) Soft Switching Capability

The ZVS boost converter act as an active clamp network, which is not connected to the input side but the output side. The soft switching characteristics are similar to achieve active clamp circuit. A main switch Q_1 has a load-dependent ZVS condition relying on the value of the leakage inductor $L_{\rm lkg}$, whereas an auxiliary switch Q_2 has a wide ZVS load range resulting from a large boost inductor $L_{\rm m}$. Thus, all switches can be turned on under ZVS condition if the energy stored in $L_{\rm lkg}$ is sufficient.

However, since ZVS condition of Q_1 is load-dependent and lost at a light load due to the insufficient loss is inevitable. To improve the efficiency even at a light load, the pulse width modulation control is used which can recover the ZVS of Q_1 . *III (d) Circuit Operation*

The switches Q_1 and Q_2 are turned ON and OFF alternatively. Due to the VDR , the circuit acts as a conventional forward converter when the switch Q_1 is turned ON and a flyback-boost converter when Q_1 is turned OFF. At the boosting phase, when Q_1 is turned ON, the transferred current through a transformer charges a link capacitor C_b . At the powering phase, when Q_1 is turned OFF, C_b is discharged.

When switch Q_1 is turned OFF, the current $I_{lkg}(t)$ charges the junction capacitor of Q_1 to V_{C01} and discharges that of Q_2 to 0 V in a short time. After the junction capacitor Q_1 is charged to V_{C01} , the antiparallel diode of Q_2 is conducted. Thus, no protection circuit is required, and the primary conduction loss can be reduced by using lower voltage –rated power switches. The conducting antiparallel diode provides the zero voltage across Q_2 until it is turned ON.

The switch Q_2 , is turned ON under ZVS conditions and the diode D_{01} is reverse biased. The transferred current via the transformer charges the junction capacitor of D_{01} to V_{C02} and discharges that of D_{02} to 0V for a short time respectively. After completing the voltage transition from D_{02} to D_{01} , the D_{02} is conducted and C_b is discharged. The current $I_{lkg}(t)$ changes its direction from positive to negative and keeps negative slope until the switch Q_2 is turned OFF. The current $I_{lkg}(t)$ flows back to input source.

After the switch Q_2 is turned OFF, the primary leakage current $I_{lkg}(t)$ charges the junction capacitor of Q_2 to V_{C01} and discharges that of Q_1 to 0V respectively. After the junction capacitor of Q_2 is charged to V_{C01} , the anti parallel diode of Q_1 is conducted. The current I_{lkg} is linearly increased. This

increasing current also provides the current snubbing effect of $\mathrm{I}_{\mathrm{D02}}$

Now, the switch Q_1 is turned ON under ZVS condition. The current I_{lkg} increases until it reaches the magnetizing current I_{Lm} . The transferred current via the transformer charges the junction capacitor of D_{02} to V_{C02} and discharges that of D_{01} to 0 V for a short time, respectively.

TABLE 1 CIRCUIT PARAMETERS

Input Voltage, V ₁	12 V
Output Voltage, V ₀	86.5V
Magnetizing Inductor, L _m	280e ⁻⁶ H
Leakage Inductor, L_{lkg}	10e ⁻⁶ H
Output Capacitors, C ₀₁ and C ₀₂	10e ⁻⁶ F
Proportional Gain, Kp	25
Integral Gain, Ki	12
Derivative Gain, Kd	0.05

IV. CONTROL STRATEGY

Two control strategies were discussed in this paper. They were pulse width modulation technique and PID control technique.

IV (a) Pulse Width Modulation Technique

To improve the output voltage, focused on reducing the switching losses, several methods are proposed. These techniques can be classified into two categories: The quasi resonant technique and the active clamp technique. To achieve the ZVS of the main switch at any load condition, a variable frequency control by adjusting the off-time with complementary gate signals has been proposed [39]. Since the auxiliary switch is turned ON for a short time before the main switch is turned ON, the recycled leakage energy can be used to achieve the ZVS of the main switch, which reduces the circulating energy effectively compared to the conventional complementary switching techniques.

The proposed light load pulse width modulation control is used in order to improve the output voltage and to reduce switching loss during light load condition. The PWM technique is used to generate signals or pulses for turning the switches ON or OFF. In PWM converters the control circuit regulates the output by fixing the switching frequency and varying the ON time of the switch. In this the output signal is compared with a carrier signal and generates a pulse, which is used to drive the switches.

IV (b) PID control law

In order to regulate the output voltage, voltage mode controller is used. The voltage mode control executes the PID control law. A PID controller is a generic control loop feedback mechanism widely used in industrial control systems. A PID controller attempts to correct the error between a measured process variable and a desired set point by calculating and then outputting a corrective action that can adjust the process accordingly.

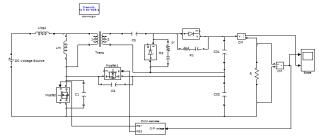
The proportional term makes the change in output that is proportional to the current error value. The proportional response can be adjusted by multiplying the error by a constant value, Kp called as proportional gain.

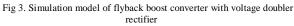
The integral term causes the steady-state error to reduce to zero, which is not the case for proportional-only control in general. The integral term is proportional to both the magnitude of error and the duration of the error. The magnitude of the contribution of the integral term to the overall control action is determined by the integral gain Ki.

The rate of change of the process error is calculated by determining the slope of the error over time and multiplying this rate of change by the derivative gain Kd. The lack of derivative action may make the system steadier in the steady state. This is because derivative action is more sensitive to higher-frequency terms in the inputs. Without derivative action, a PI-controlled system is less responsive to real and relatively fast alterations in state and so the system will be slower to reach set-point and slower to respond to perturbations than a well-tuned PID system. Hence a PID control law is used.

V. SIMULATION

The simulation of the flyback boost converter with voltage doubler rectifier is done using MATLAB and it is shown fig 3.





In this two converters are designed. One is boost converter and the other is flyback converter. The MOSFET switch 1 and the magnetizing inductor L_m is common for both boost converter and flyback converter. The VDR circuit is also designed to regulate the output voltage. The load is connected across the output capacitors in parallel manner. The output voltage is fed as input to the PWM controller. The PWM controller generates the pulses to drive the MOSFET switches. Table 1 describes the parameters for the various components used in the simulation circuit.

A subsystem is created for the control process. The output voltage is given as the input to the subsystem. Inside the subsystem the PID control law and PWM controller are present. The output voltage and the reference voltage are summed together and it is given to the PID controller. The regulated output voltage is fed as input to the PWM controller. The PWM controller compares the input signal with a carrier signal and generates output signal which is demuxed and used as pulses for two switches.

VI. SIMULATION RESULTS The input given is 12 V which is shown in fig 4.

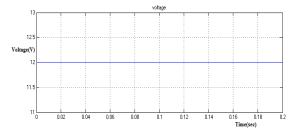


Fig 4. Input voltage waveform

For 10 ohm load the output voltage is 86.5 V and the output current is 8.65 A. The output voltage and current waveforms are shown fig 5.

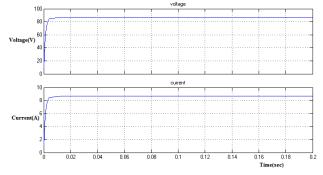


Fig 5. Output waveform for 10 ohm load

Thus even at the light load condition the output voltage is stepped up appropriately without any distortions or losses.

VII. CONCLUSION

Non isolated high step up DC-DC converter with pulse width modulation technique is presented in this paper. The common parts between the boost converter and the flyback converter are integrated together. The voltage doubler rectifier is used to step up the voltage. In addition the ZVS technique which is used to achieve soft switching and PWM technique which is used to improve the output voltage during light load condition is also discussed to discuss ZVS load range. This simple and effective technique gives many desirable features for high efficiency and high step-up applications. An improved technique to enhance the step up capability and to improve the output voltage during light load condition is proposed and discussed in this paper. Therefore the proposed converter topology and control technique can be a promising solution for high step-up applications.

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