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*Original Article*

# Analysis and Optimal Design of Power-Efficient and High-Stable Proposed SRAM Cell

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***Abstract*** *- Power dissipation is the key challenge of today's IC design, which reduces the lifetime of battery-operated devices. Continuous scaling of CMOS technology reduces the channel length and increases the static power dissipation. Leakage is the dominating factor in memory design which contributes almost 40-50% of overall power dissipation. In today's high-performance design, leakage power is almost equal to dynamic or switching power. Almost 40% or more of total power consumption is due to the leakage power of the transistor, and this factor is increasing day by day with the scaling of technology until some effective methods are introduced for leakage controls. Memory designs require a good noise margin for the stability of SRAM cells. Higher the value of noise margins higher the speed of SRAM cells. The main aims of this study are to simulate various topologies of 10T and 6T SRAM cell design using CMOS and FinFET technology and evaluate their performance for comparisons. Different techniques are applied for power reduction at lower operating voltage. Evaluated results are also compared with 6T SRAM cells for a better understanding of the results. There is 37%, 73% and 19% improvement in HSNM, RSNM, and WSNM, respectively, in 10T SRAM cells compared to conventional 6T cells. HSPICE tool at 32nm technology is used for simulation.*

***Keywords*** *- CMOS, FinFET, HSNM, MTCMOS, SCE.*

## 1. Introduction

With the continuous scaling of technology, leakage current dominates even when the transistors are in OFF condition. Static power dissipation at the lower technology node becomes more dominant than dynamic one. In our electronic systems, the memory subsystem is one of the major parts because it occupies a large portion of the circuit. Leakage power has an adverse effect on the memory design circuit. Earlier, memory was designed using CMOS technology. However, as the CMOS technology is scaled down to a lower node, many issues are created, such as Short Channel Effects (SCE), sub-threshold leakage current, reverse-biased junction leakage current, Drain-Induced Barrier Lowering (DIBL), Gate-Induced Barrier Lowering (GIBL) [1]. Out of all issues, sub-threshold leakage and gate leakage current play an important role in SRAM cells. The researchers proposed various methods in earlier times to reduce the leakage current, out of which Multi-Threshold (MTCMOS) and Variable Threshold (VTCMOS) are traditional methods.

MTCMOS has the demerits of having many fabrication steps and does not retain data in standby mode, whereas VTCMOS requires a separate pin to generate bias voltage levels. However, one of the major drawbacks of both techniques is the large size and delay. Researchers mostly use voltage scaling for leakage power reduction [2]. The famous relation of power and supply voltage of proportionality plays an important role in reducing power with the scaling of voltage [3]. When the SRAM is operated at a sub-threshold level, there is a possibility of threshold voltage ($V_{th}$) variation because, in deep-submicron technology [4], a progressive increase in $V_{th}$ variance has a negative impact on SRAM stability.

Further, some new device structures were introduced to resolve these memory issues, including SOI (Silicon on Insulator) MOSFET, double gate structures, CNT (Carbon nanotubes) field-effect transistors, quantum dot devices, etc. Tunneling field effect transistors (TFETs) devices are also able to solve the issues of CMOS with the properties of having low power, more density, and better performance [5]. But at the time of operation in the SRAM cell, it was ineffective in preventing data retention because of SNM reduction [5]. Double Gate (DG) is mostly preferred among all these structures because of their compatibility with the circuits. In DG structures, the features of electrical coupling of the front and back gates help reduce SCE, DIBL, and GIBL. The use of FinFETs structures in the industry overcomes all the issues related to CMOS. FinFETs can either have an independent gate structure, in which the front and back gates are used separately, or a tied gate structure, in which both are shorted. In FinFET, there is good gate control over the channels, which


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helps reduce SCE. To improve gate control, these gates are built so that they wrap around the channel.

One of the key challenges in the SRAM cells is the problem of data stability degradation and power leakage. However, one of the major issues with SRAM has been identified as data stability in the Extremely Low Voltage Transfer Methodology [6]. The design of SRAM cells using FinFET eliminates all the problems CMOS technology faces, and it is highly desirable to improve data stability and performance [7]. The reduced SCE and leakage current feature of FinFET makes it suitable for future nanoscale memory circuit design [8]. It is noticed that power dissipation is also affected by the temperature for both storing and restoring operations [9]. Store operations are more affected by temperature changes as compared to restore operations [9]. However, in our calculations, we have not considered the temperature effect.

Due to its straightforward and compact form, the traditional 6T SRAM cell is utilized, shown in Figure 1, with four transistors acting as two coupled back-to-back inverters and the remaining two serving as access transistors. This cell has the problem of power dissipation and stability in the ON state of the cell [10]. Many cells are designed by increasing the number of transistors for better performance at ultra-low voltage operations. The decreasing feature sizes of cells improve stability and performance and also reduce the operating voltage, making it important to have clear comparisons under an iso-area condition [11]. The design of SRAM cells by using multi-threshold voltage also helps to achieve highly stable and low-power memories [12]. The effective way to change threshold voltage is to change the flat-band voltage because they are proportional to each other [12].

In comparison to other SRAM cells that have been created, the suggested cell has an enhanced SNM and uses less power [13]. Lowering the power consumption of SRAM helps reduce the overall dissipation of power of devices [14, 15]. Figure 2 represents CMOS-based 10T SRAM having ten transistors in which six transistors are the same as the conventional cells. For successfully active operations, bit lines and word lines are turned ON. Two additional access transistors are present on either side of the cell used to transfer data from bit-lines to the node and affect writing ability [16]. The ground lines for all transistors have a common connection with $V_{GND}$ [16].

Downscaling of $V_{DD}$ is a well-liked strategy to achieve power efficiency in SRAM architecture because dynamic or active power declines quadratically with a decrease in supply voltage ($V_{DD}$). Static power, which accounts for a sizeable portion of total power dissipation, decreases linearly with decreasing $V_{DD}$ [7]. Scaling the supply voltage thereby lowers the overall power dissipation of SRAM cells. In contrast, operation delay increases with $V_{DD}$ downscaling, considerably increasing total energy per read/write cycle. When the noise margin significantly reduces, the circuit is more vulnerable to operational failure. Building an SRAM cell that can successfully navigate the aforementioned challenges and perform reliably is essential for realizing a power-efficient accelerator memory.

Cell stability, read failures and cell access time failures are all important problems with SRAM reliability. Performance deterioration caused by reliability during operation cannot be overlooked with technological scaling. Sub-threshold leakage is a result of technology scaling, and short channel effects, gate dielectric leakage, and device-to-device variances all contribute to this leakage. It is impossible to avoid studying FinFET structure when designing SRAM cells. Although the FinFET 2D/3D model has been suggested in various research articles, a thorough analysis of how variations in process parameters, temperature, device structure, etc., affect output characteristics has not been done. Leakage issues with FinFET are the subject of very few research papers. For FinFET devices, band-to-band tunnelling (BTBT) and edge-direct tunnelling (EDT) have been investigated. Few research papers are aware of the field of process variation of SRAM cell design using FinFET. There has not been a proposed advanced cell for a FinFET-based structure yet. In-depth research on improved SRAM cells, such as the 7T, 8T, 9T, 10T, and 12T, would be necessary for low-power applications in all FinFET structure scenarios. Very few studies have been conducted at the subsystem level on FinFET-based SRAM cells for process variation and temperature impacts. The majority of publications base their research on bulk MOSFET and DG MOSFET fabrication and process technology for SRAM cell design. Numerous articles have calculated the static noise margin (SNM), but none have documented how it varies depending on the construction and process factors of the devices. Since FinFET is novel and has a complex structure, no research study has reported on creating any precise models.

Conventional 6T cells face the issue of the delayed read operation, which means the time taken to respond to an operation is quite large, resulting in the increased value of leakage power dissipation. The cell is unsuitable for practical applications due to its decreased performance. The decrease in supply voltages also lowers the SNM of this cell. Reduction in supply voltages leads to problems of data corruption, delay in the reading operation, and invalid data sensing from the cell, which is undesirable for practical applications. Higher values of supply voltage increase leakage power, which is also unacceptable. After encountering so many drawbacks with the 6T SRAM, a new cell was proposed in which one extra transistor is added to the regular SRAM cells' ground path to lessen leakage during standby mode.

Additionally, there was no improvement in the cells' read speed with the planned 7T SRAM cell arrangement. The

performance and stability of the aforementioned 6T and 7T SRAM cells are influenced by transistor design. It is possible to gauge the stability of a cell by looking at the ratio (β) between the sizes of the pull-down and access transistors. Although a higher value improves stability, it is counterbalanced by a higher leakage power and area. An 8T fixed the issue of data loss during read operations. To lower power consumption and boost data stability, a 9T SRAM cell was used. This cell also has some challenges in reducing leakage current because the cell is ON even in an idle state. To overcome the above limitations, a 10T SRAM cell is proposed.

## 2. Literature Review

All the parts of a computer or other electronic system are combined into a single integrated circuit (IC) to form a system-on-chip. In modem SOCs, memories can take up to 70% of the overall chip area. The various transistor combinations (6T, 7T, 8T, etc.) are used because of their greater performance capabilities and compatibility with the CMOS logic process. For many SOC-embedded memories, SRAM has become the workhorse. With CMOS processes, the cell has scaled well and has even evolved into a tool for describing and contrasting various processes. However, memory cells are more vulnerable to process variation and ageing effects as devices get smaller, leading to higher failure rates.

A literature review is a crucial component of every research project. Some earlier methods and their significance for generating SRAM cells and fresh ideas for creating new cells are discussed in this section. Additionally, other factors are looked at when developing new cells for low-voltage applications.

Singh et al. [17] suggested a novel approach to decrease power consumption and improve read operation stability. In this case, a CMOS device with a 180nm technology node creates the SRAM cell. Compared to ordinary 6T cells, the overall power dissipation is lower. The authors calculated both types of power dissipation. Additionally, noise margins are computed for various temperature ranges and supply frequencies. The suggested cell is employed in memory applications requiring extremely low power and great stability at the lower voltage.

In [18], a model cell with high speed and low power consumption was suggested. Using the HSPICE tool, Gsoliv and Gujar created 6T and 12T SRAM cells at the 130nm, 90nm, and 65nm technology nodes. It is suggested that the 12T SRAM cell is contrasted with a load-free 6T SRAM. When the findings were compared, the 12T cell had reduced area and power consumption, so the fabrication method does not need to be altered. This cell is utilized in stand-alone SRAM applications as well as chip caches in embedded tips, logic devices, and stand-alone SRAM applications.

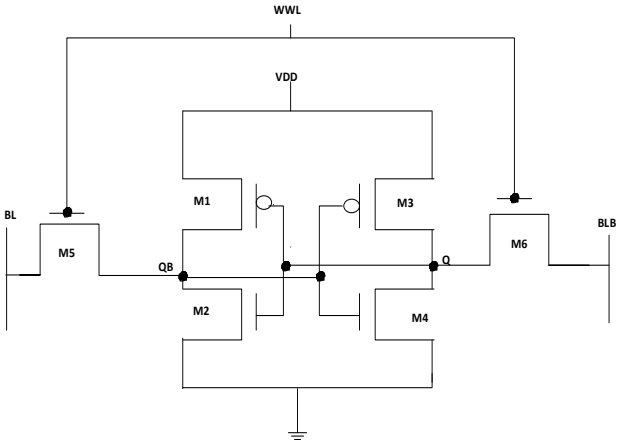


**Fig. 1 6T SRAM cell [16]**

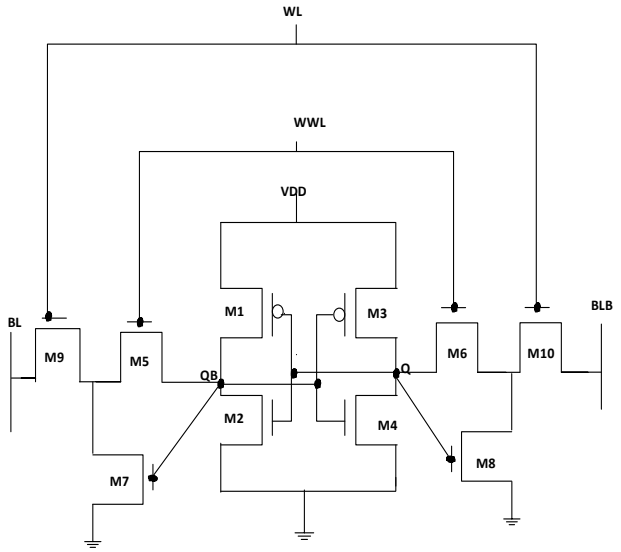


**Fig. 2 10T CMOS-based cell [16]**

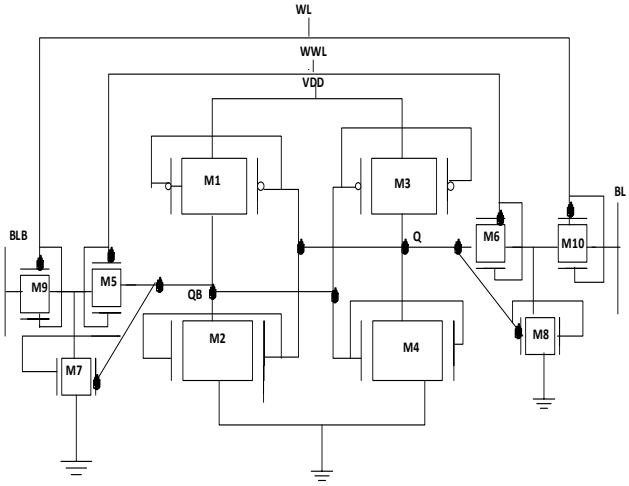


**Fig. 3 Proposed-1 cell**

Islam and Hasan [19] put up a novel technique to construct low-power, changeable SRAM cells. Stacking offset, which is achieved using read buffers and tail transistors coupled in series, accounts for the low power dissipation. In their investigation, they compared Schmitt trigger-based SRAM cells and 6T, 9T, and other types. Leakage power dissipation, read access time and its variability, write stability, and read stability were among the measures they compared. Current or static power was not discussed. These cells' ability to be used for low-power applications in scaled technology while PVT variations are present is one of their advantages.

A unique 10T SRAM cell suggested in [20] reduces power dissipation by making use of the sleep transistor stacking effect. The authors extend the pull-down and pull-up paths with two sleep transistors to reduce leakage during read and write operations on the cell. There is a significant power decrease in the cell even though there are four more transistors than in ordinary 6T SRAM cells. Dynamic power dissipation is also decreased by making the wordline and bitlines shorter. The 65nm technology node CMOS chip used to construct the 10T SRAM cell has a supply voltage of 1.2V. Comparing the 10T SRAM cell's simulation results to those of traditional 6T cells.

A 10T SRAM cell was presented by Rohit Lorenzo et al. [21] in order to overcome the difficulties of stability, power, and half selected. Comparing the proposed cell to 7T, 11T, and 9T SRAM cells. The suggested cell has a large read and writes power decrease when compared to 11T and 9T cells. Applications requiring less power use the cell. The 10T cell's architecture decreases write stability degradation while doing away with the half-select issue.

In order to achieve the objectives of good read stability, smaller space, and low power consumption, a 1-bit 10T SRAM cell is designed [22]. Traditional 6T SRAM cells have exhibited subpar read and write operation stability levels. To solve the read stability issue, alternative cell configurations, including 7T, 8T, 9T, and 10T, have been developed. However, these designs raise the stability value at the expense of raising the power dissipation value. Authors have developed a brand-new 10T SRAM cell to address the abovementioned issues. The transmission gates are used by the cell as a stacking effect. The cell was put into use on nodes using 180nm technology and a 1.8V supply.

In [23], a twin gate FinFET was used to construct a standard 6T SRAM cell. The developed cell is compared to 6T CMOS SRAM cells at technology nodes of 45nm, 32nm, and 16nm. The static noise margin value has increased due to the FinFET-based SRAM cell. Both AC and DC parameters are used to compare the outcomes of the two cells. For the purpose of reducing leakage power, a hybrid circuit was designed [24]. The circuit's fundamental logic is based on power gating and biassing. The hold-state hybrid circuit and other current low-power solutions were compared. Leakage power and SNM are used as the basis for comparison. At a 32nm technology node, Symica DE is used for all simulations. In comparison to ordinary 6T cells, hybrid circuits have lower leakage power values while retaining good stability.

## 3. Proposed FinFET-based SRAM Cell

The excellent features of CMOS, having the lowest static power dissipation and compatibility with multiple circuit configurations, make it used in SRAM cells. Also, CMOS cells have better noise immunity and speed, but below 45nm nodes have problems with increased short-channel effects and random dopant fluctuations. The multi-gate structure feature of FinFETs makes them the most suitable candidate for SRAM design. In FinFET SRAMs, parameters optimization such as $V_{DD}$, Fin height ($H_{fin}$), and $V_{th}$ are necessary for reducing leakage [25]. But the stability of SRAM cells is affected by the reduction in $V_{DD}$. The design of SRAM using FinFET proves improved performance compared to CMOS in earlier work [25]. For FinFET-based SRAM, two considerations, functionality and tolerance to process variation, become more prominent, and for this, it is necessary to design a cell with the correct SNM [25].

FinFETs are built using either a shorted gate or an independent gate construction. The Shorted or the Tied gates FinFET has shorted gates to improve the short channel effect, while the independent gate has one gate that acts as a switch ON/OFF, and the remaining gates are used to control the threshold voltage [46]. The two front and the back gates of DG- FinFET help in reducing the problems of data stability and power consumption [27]. In this paper, the short gate DG-FinFET SRAM cell is analysed, named as proposed-1 circuit as shown in Figure 3, and the results are compared to CMOS-based SRAM.

### *3.1. Read Operation*

The first step is to charge bitlines and wordlines at $V_{DD}$ and write word lines (WWL) to the ground. Turning OFF- WWL cuts the connection of access transistors with the cell to eliminate the disturbance caused by bit lines [20]. As shown in Figure 3, both the transistors M8 and M7 work to act as reading buffers. The operation can be well explained by taking the node QB to '1' so that the outside transistors M7, M9, and M10 are ON, and BLB will discharge through M9-M7 transistors for a correct read operation.

### *3.2. Write Operation*

This operation starts with the charging of both wordlines. Here we keep the voltage of the WWL higher than the supply for better write stability [28]. Both the access transistors always remain ON during this operation for writing the data from bitlines. BL and BLB are concurrently maintained at supply voltage and ground to write data "0" at node Q, and the same is true for writing "1".

## 4. Research Method

The access transistors M9-M10 and the transistors M5-M6 are cut off from the cell if neither the WL nor the WWL is asserted. Certain power reduction techniques are vital because the two cross-coupled inverters will continue storing data until the power is turned on and the leakage power increases [29]. Various power reduction techniques are utilised in this area.

### *4.1. Sleep Transistor Technique*

The fundamental idea underlying this method is the stacking effect of transistors for leakage power between the source voltage and the ground. It is considered that "a state with more than one transistor OFF in a path from the supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path"[30]. According to this method, a connection is made between the top and bottom of the cell for an NMOS and PMOS leakage control switch. Figures 4 and 5 show the proposed 2 and 3 circuits of cell design using CMOS and FinFET.

In the active mode of operation, both the additional transistors are ON, and in hold operations, they are OFF. In active mode, operations remain normal because of no change in the path between $V_{DD}$ and $V_{GND}$. The supply is cut to the cell in the hold operation to create a virtual $V_{DD}$ and $V_{GND}$ path. The value of resistance from supply to ground increases with the introduction of leakage control transistors [31]. In the OFF condition of the cell, static power is reduced with the reduction in the output to ($V_{DD}$-$V_{th}$).

### *4.2. Drowsy Cache Technique*

This approach takes advantage of various supply voltages in both active and hold modes. 50% of the supply is applied in hold operation, so the voltage reduction indicates the static power reduction. High voltage $V_{DD}$ is applied in an active mode of operation to improve the cell's performance. Since on reducing the supply leakage currents are also reduced, therefore low supply is used in standby mode [29]. Applying a low sleep signal to supply $V_{DD}$ maintains the ON state of the M11 (PMOS) transistor during active mode operation. In hold mode M12 (NMOS) transistor is ON by keeping the sleep signal high. Since NMOS has the property of passing strong '0' and weak '1', it can reduce the voltage from VDD, while PMOS has the property of passing strong '1' and weak '0', increasing the value of supply in the circuits. Figures 6 and 7 indicate the design of the proposed 4 and 5 cell circuits (CMOS and FinFET - based 10T SRAM cells using the drowsy cache technique.

### *4.3. SVL Technique*

The SVL circuit is increasingly widely used because of its good characteristics of having low power and high-speed performance [32]. The basic logic of having high operating speed and performance is producing "a supply voltage to maximum or minimum" and the "ground voltage to minimum or maximum" [32]. It is mostly applied to shorted DG-FinFET structure. This technique helps reduce both sub-threshold and gate leakage currents in the circuit.

The basic logic behind this technique is that it provides full supply ($V_{DD}$) and ground in active mode, while in standby mode, a slightly lower $V_{DD}$ and a higher ground voltage are provided to reduce leakage in the circuit. SVL switch is basically of two types upper SVL (USVL) used above the cell to reduce the supply voltage or lower SVL (LSVL) connected below the cell to increase the ground potential. SVL techniques can also be combined with USVL and LSVL switches. Here we used a combination of both switches to reduce leakage in the cell.

The USVL consists of only one PMOS switch (M13) and the series combination of two remaining NMOS switches in which both NMOS and PMOS switches are used in parallel. In active mode, the PMOS switch is ON to connect the supply $V_{DD}$ to the cell, while in standby mode NMOS switch is ON to provide the reduced supply voltage to the cell.

LSVL consists of only the NMOS switch (M14) and the series connection of two PMOS switches (M15, M16), and both are connected parallel. In the active mode, the NMOS switch is ON which connects the cell to the ground; while in hold mode, the PMOS switch is ON which connects the increased value of ground to the cell [47]. Here we combine upper and lower SVL switches to reduce leakage in the cell [34, 35, and 47]. Figure 8 and 9 shows CMOS and FinFET SRAM design using the SVL technique; here, CLK 2 and CLK 1 signals are used in USVL and LSVL to ON the switches.

Table 1 represents the operation of both switches in active and holds modes. Table 2 shows the advantages, disadvantages, and leakage power comparisons between different methods. It can be observed from the table that the SVL technique is best in reducing power and for stability improvement, but it has serious drawbacks in the area, and its implementation is also hard to compare to the remaining two techniques. As the circuits of this technique are the same as the reference [36], the values of SNM and power are modified, or we can say values are improved.

**Table 1. SRAM cell operation**

| Operations | LSVL circuit | USVL circuit |
|---|---|---|
| **Read and Write operations.** | NMOS on (VSS is supplied) | PMOS on (VDD is supplied) |
| **Hold operation** | PMOS on (VS(>VSS) is supplied) | NMOS on VD(<VDD) is supplied |

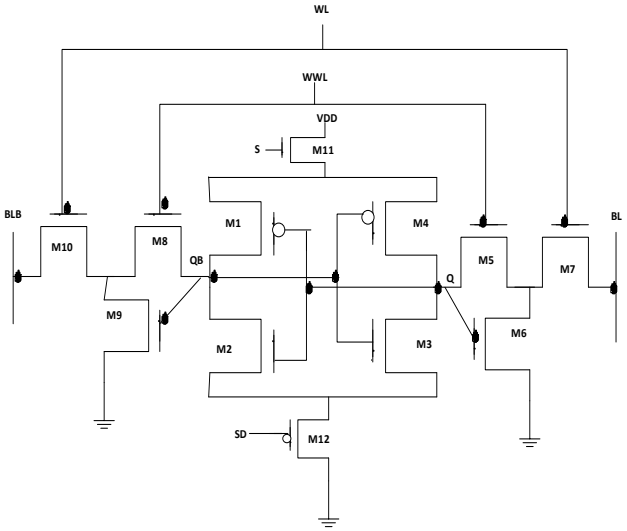


**Fig. 4 Proposed-2 cell**

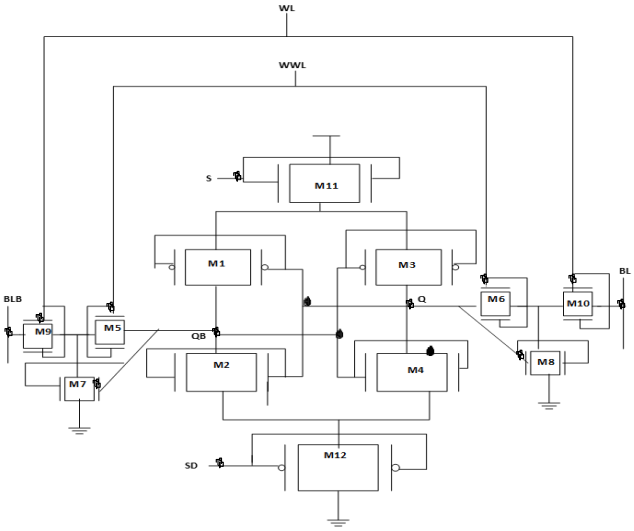


**Fig. 5 Proposed-3 cell**

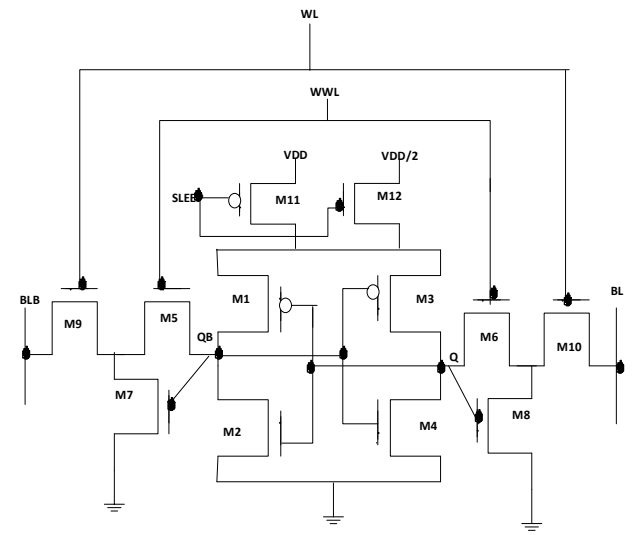


**Fig. 6 Proposed-4 cell**

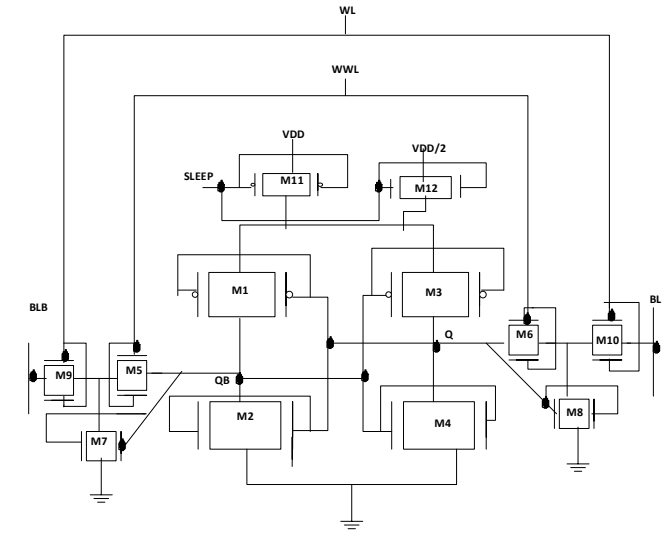


**Fig. 7 Proposed-5 cell**

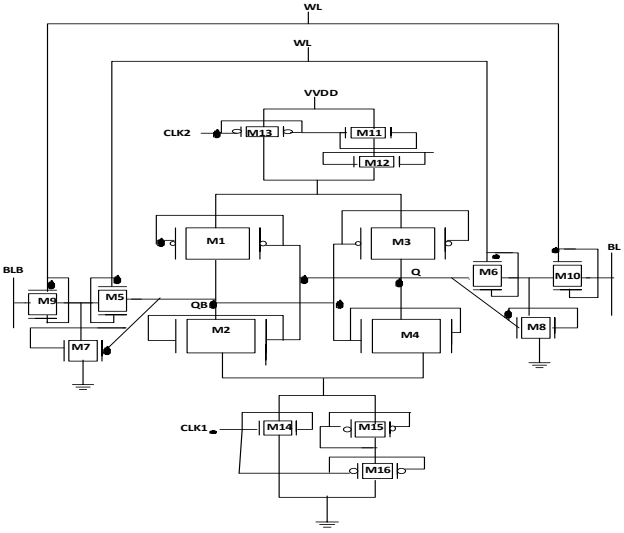


**Fig. 8 CMOS cell using SVL Technique [28]**

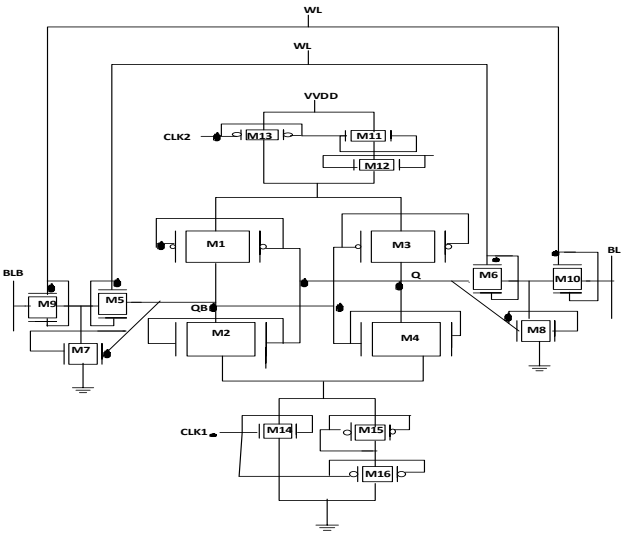


**Fig. 9 FinFET cell using SVL Technique [28]**

## 5. Simulation Results

### *5.1. Static Noise Margin*

The capability of the cell to tolerate dc noise defines its stability and is calculated by soft error rates [37]. Static noise margin is a measure that is frequently used to determine how stable an SRAM cell is. With the change in operating conditions and environmental variations, a dc disturbance is created in the form of static noise. There are several methods for calculating noise margin, one of which is a graphical approach. The voltage transfer characteristics (VTC) of the inverters are first drawn, followed by an inverted VTC curve of the same inverters. These two curves are then joined to form a butterfly-shaped curve, and the "largest-sized square which will fit inside the curve" is found. The value of SNM is the side of the square. The second way to calculate SNM is by applying a dc noise on the storage nodes of opposite polarities and saving the voltage [38]. Here we use the butterfly curve method for SNM calculations.

### *5.2. Hold SNM*

From the observations, it was found that in RAM cells, both SNM and supply voltage are correlated or proportional to each other. The variations between the different values of supply voltages and noise margins are summarized in Table 3. Noise margin and supply voltages are proportional to each other for all operations, as shown in Table 4, because the effect of noise in the circuit becomes more significant when the supply voltage goes down [39]. Therefore, voltage is scaled to limited levels such that the expected dc noise is smaller than the noise margin. In inverters, the supply voltage defines the maximum voltage or voltage swing at the output nodes [39]. With carefully observed, it can be said that there is an improvement of 1.6x over 10T CMOS SRAM cell, 1.2x over proposed-1 cell and 1.4x over CMOS cell using SVL technique when designed SRAM cell with FinFET technology using SVL technique. It is clearly observed from the tables that as the number of transistors in the cell increases, the value of SNM also increases to 37%.

### *5.3. Read SNM*

It is commonly acknowledged that supply voltage has an impact on stability. The supply voltage value should be high for the large value of SNM [22]. Table 5 shows the values of RSNM for 10T SRAM cells at different supply voltages. When designing SRAM cells with FinFET technology, it is possible to conclude from several findings that there is an improvement of 2.1x over CMOS-based 10T SRAM cell, 1.52x over proposed-1 cell, 1.4x over proposed-3 cell, and 1.1x over CMOS cell utilising SVL approach. RSNM for 6T CMOS -based cell is 180mV whereas, for FinFET- based SRAM cell, it is 220mV. There is a 73% improvement in RSNM from 6T to 10 T SRAM cells.

### *5.4. Write SNM*

The cells WSNM refers to its capabilities to write data to the storage node. WSNM for a 10T CMOS design cell is 210 mV, while WSNM for a 32nm FinFET design cell is 225 mV when VDD = 900 mV. The values of WSNM for 10T SRAM cells at various supply voltages are shown in Table 6, along with a comparison. The proposed cells' butterfly curve is depicted in Figure 10. Measurements show improvements of 1.4x over CMOS-based 10T SRAM cells, 1.1x over proposed-1 cells, 1.04x over proposed-3 cells, and an enhancement 1.4x over those cells when SRAM cells employing FinFET technology are built using the SVL technique. Performance in FinFET-based cells has improved. From the tables, we can see that as we go from 6 to 10 transistors, the values of SNM also grow, reaching a maximum of 19%. The SNM improvement of the suggested cell compared to other cells is shown in Table 9.

**Table 2. Comparison between methods**

| Technique | Advantages | Disadvantages | Number of transistors | Reduction in leakage power w.r.t. FinFET based 10T SRAM cell |
|---|---|---|---|---|
| **Sleep transistor** | Easy implementation | Low stability | 12T | 79.43% |
| **Drowsy cache technique** | Easy implementation<br>High switching speed<br>More power reduction than drowsy cache and sleep transistor techniques | Low stability<br>Uses Two Supply Voltage | 12T | 98.81% |
| **SVL Technique** | High stability<br>Effective for leakage and static power reduction | Area overhead<br>Large delay | 16T | 95.52% |

**Table 3. SNM analysis for 6T SRAM cells**

| Parameter | SRAM Cells | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SNM | HSNM | | | | RSNM | | | | WSNM | | | |
| Supply Voltage | CMOS SRAM | FinFET SRAM | CMOS SRAM using SVL Technique | FinFET SRAM using SVL Technique | CMOS SRAM | FinFET SRAM | CMOS SRAM using SVL Technique | FinFET SRAM using SVL Technique | CMOS SRAM | FinFET SRAM | CMOS SRAM using SVL Technique | FinFET SRAM using SVL Technique |
| 900mV | 160mV | 185mV | 190mV | 235mV | 150mV | 160mV | 180mV | 220mV | 100mV | 150mV | 170mV | 190mV |
| 800mV | 145mV | 160mV | 170mV | 220mV | 130mV | 150mV | 165mV | 200mV | 80mV | 130mV | 155mV | 170mV |
| 700mV | 130mV | 145mV | 150mV | 195mV | 110mV | 135mV | 150mV | 180mV | 65mV | 125mV | 140mV | 150mV |
| 600mV | 110mV | 125mV | 120mV | 180mV | 90mV | 120mV | 120mV | 160mV | 50mV | 110mV | 115mV | 130mV |
| 500mV | 90mV | 105mV | 90mV | 150mV | 70mV | 105mV | 90mV | 130mV | 40mV | 90mV | 90mV | 110mV |
| 400mV | 75mV | 90mV | 50mV | 120mV | 50mV | 85mV | 55mV | 100mV | 30mV | 60mV | 60mV | 70mV |
| 300mV | 55mV | 70mV | 40mV | 85mV | 30mV | 55mV | 40mV | 80mV | 20mV | 40mV | 30mV | 50mV |
| 200mV | 30mV | 45mV | 40mV | 50mV | 10mV | 30mV | 30mV | 60mV | 10mV | 20mV | 20mV | 35mV |

**Table 4. Hold SNM analysis for 10T SRAM cells**

| Parameter | SRAM Cells | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | CMOS SRAM [16] | Proposed-1 | Proposed-2- | Proposed-3 | Proposed-4 | Proposed-5 | CMOS cell using SVL Technique [28] | FinFET cell using SVL Technique [28] |
| 900mV | 190mV | 250mV | 230mV | 280mV | 120 mV | 130 mV | 360mV | 380mV |
| 800mV | 150mV | 220mV | 200mV | 250mV | 100 mV | 110 mV | 300mV | 300mV |
| 700mV | 130mV | 190mV | 180mV | 200mV | 85 mV | 95 mV | 280mV | 280mV |
| 600mV | 110mV | 150mV | 150mV | 180mV | 70 mV | 85 mV | 230mV | 250mV |
| 500mV | 90mV | 120mV | 100mV | 150mV | 55 mV | 70 mV | 200mV | 200mV |
| 400mV | 70mV | 90mV | 80mV | 130mV | 45 mV | 55 mV | 150mV | 180mV |
| 300mV | 50mV | 70mV | 50mV | 80mV | 35 mV | 40 mV | 100mV | 150mV |
| 200mV | 30mV | 40mV | 30mV | 50mV | 20 mV | 25 mV | 80mV | 80mV |

**Table 5. Read SNM analysis for 10T SRAM cells**

| Parameter | SRAM Cells | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | CMOS SRAM [16] | Proposed-1 | Proposed-2 | Proposed-3 | Proposed-4 | Proposed-5 | CMOS Cell using SVL Technique [28] | FINFET Cell using SVL Technique [28] |
| 900MV | 190MV | 240MV | 190MV | 260MV | 200 MV | 210 MV | 220MV | 320MV |
| 800MV | 180MV | 210MV | 180MV | 210MV | 180 MV | 190 MV | 200MV | 300MV |
| 700MV | 170MV | 200MV | 170MV | 200MV | 150 MV | 170 MV | 180MV | 280MV |
| 600MV | 160MV | 190MV | 160MV | 190MV | 130 MV | 150 MV | 160MV | 250MV |
| 500MV | 150MV | 170MV | 150MV | 170MV | 100 MV | 120 MV | 130MV | 220MV |
| 400MV | 120MV | 150MV | 120MV | 150MV | 80 MV | 100 MV | 110MV | 180MV |
| 300MV | 100MV | 80MV | 100MV | 80MV | 60 MV | 80 MV | 80MV | 150MV |
| 200MV | 50MV | 50MV | 50MV | 50MV | 30 MV | 40 MV | 50MV | 100MV |

**Table 6. Write SNM analysis for 10T SRAM cells**

| Parameter | SRAM Cells | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | CMOS SRAM [16] | Proposed-1 | Proposed-2- | Proposed-3 | Proposed-4 | Proposed-5 | CMOS cell using SVL Technique [28] | FinFET cell using SVL Technique [28] |
| 900mV | 150mV | 200mV | 180mV | 220mV | 180 mV | 200 mV | 210mV | 225mV |
| 800mV | 130mV | 180mV | 170mV | 210mV | 160 mV | 180 mV | 190mV | 200mV |
| 700mV | 110mV | 150mV | 140mV | 190mV | 120 mV | 150 mV | 160mV | 180mV |
| 600mV | 90mV | 130mV | 120mV | 160mV | 100 mV | 110 mV | 120mV | 150mV |
| 500mV | 70mV | 100mV | 90mV | 120mV | 80 mV | 70 mV | 100mV | 120mV |
| 400mV | 50mV | 80mV | 70mV | 90mV | 60 mV | 50 mV | 75mV | 100mV |
| 300mV | 30mV | 50mV | 50mV | 60mV | 40 mV | 30 mV | 40mV | 70mV |
| 200mV | 10mV | 30mV | 30mV | 40mV | 20 mV | 10 mV | 20mV | 40mV |

**Table 7. Static Power analysis for 6T SRAM cell**

| Parameter | SRAM Cells | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | CMOS SRAM [16] | Proposed-1 | Proposed-2- | Proposed-3 | Proposed-4 | Proposed-5 | CMOS cell using SVL Technique [28] | FinFET cell using SVL Technique [28] |
| 900mV | 34.459µW | 16.559nW | 16.483nW | 7.745 nW | 4.483 nW | 264.687pW | 15.838nW | 1.476nW |
| 800mV | 21.941µW | 12.221nW | 12.244nW | 3.756nW | 2.236 nW | 175.209pW | 11.562nW | 840.731pW |
| 700mV | 12.869µW | 8.742nW | 1.754nW | 1.810nW | 2.734 nW | 114.149pW | 8.180nW | 480.357pW |
| 600mV | 5.932µW | 6.007nW | 1.259nW | 857.313pW | 1.059 nW | 72.819pW | 5.560 nW | 272.901pW |
| 500mV | 1.724µW | 3.910nW | 859.979pW | 395.203pW | 658.672pW | 45.123 pW | 3.580nW | 151.864pW |
| 400mV | 264.334nW | 2.356nW | 546.717pW | 175.33pW | 445.611pW | 26.796 pW | 2.1354nW | 81.226 pW |
| 300mV | 24.304nW | 1.261nW | 311.510pW | 72.958 pW | 301.515pW | 14.871 pW | 1.152nW | 40.533 pW |
| 200mV | 1.536nW | 548.267pW | 146.812pW | 26.976pW | 123.414pW | 7.282 pW | 534.176 pW | 17.713pW |

**Table 8. Static power analysis for 10T SRAM cell**

| Parameter | SRAM Cells | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Supply Voltage | CMOS SRAM [16] | Proposed-1 | Proposed-2- | Proposed-3 | Proposed-4 | Proposed-5 | CMOS cell using SVL Technique [28] | FinFET cell using SVL Technique [28] |
| 900mV | 27.4333µW | 18.0924µW | 17.6491µW | 7.7448 nW | 3.0891nW | 233.676pW | 12.5842nW | 1.0887nW |
| 800mV | 21.1726µW | 14.1714µW | 8.4183µW | 3.7563nW | 2.3536 nW | 173.254pW | 9.2554 nW | 644.2810pW |
| 700mV | 15.6591µW | 10.5399µW | 50.9286µW | 1.8101nW | 1.7544 nW | 112.138pW | 6.5865 nW | 376.9662pW |
| 600mV | 10.8979µW | 7.1964µW | 80.102µW | 857.3134pW | 1.2596 nW | 70.717pW | 4.4924 nW | 217.1381pW |
| 500mV | 6.8848µW | 4.2872µW | 1.6651µW | 395.2036pW | 859.9792pW | 40.132pW | 2.8951 nW | 122.3169pW |
| 400mV | 3.6126 µW | 2.0070µW | 183.1664nW | 175.3316pW | 546.7171pW | 24.702pW | 1.7219 nW | 66.5833 pW |
| 300mV | 1.1944 µW | 531.1590nW | 90.3695nW | 72.9579 pW | 311.5105pW | 12.671pW | 905.4496W | 34.1698 pW |
| 200mV | 142.770nW | 16.5592nW | 40.007 nW | 26.9760 pW | 146.8124W | 6.2527 pW | 383.8614W | 15.5684 pW |

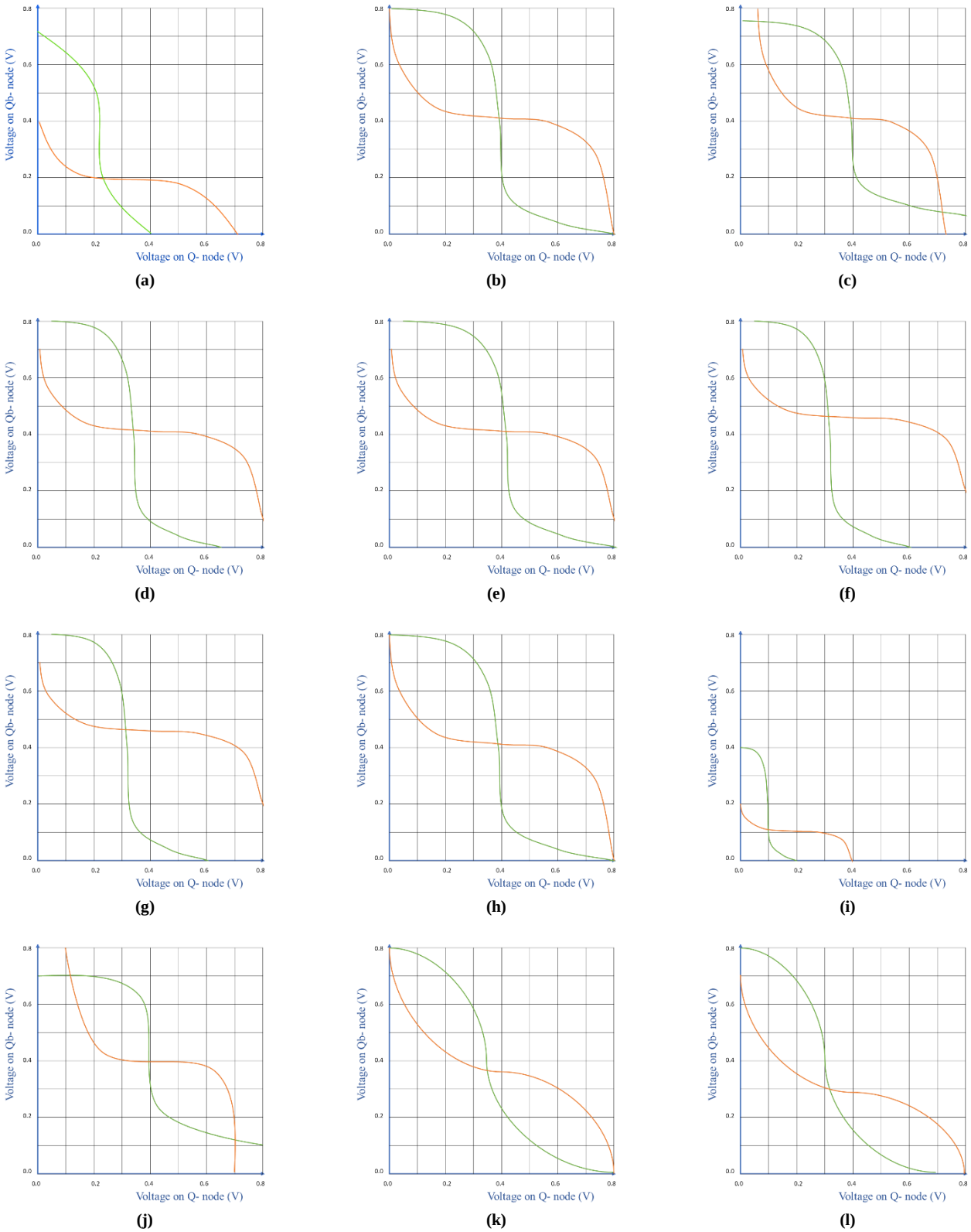


**Fig. 10 (a) CMOS HSNM (b)CMOS RSNM (c)Proposed-1 HSNM (d)Proposed-1 RSNM (e) Proposed-2 HSNM (f)Proposed-2 RSNM (g) Proposed-3 HSNM (h)Proposed-3 RSNM (i) Proposed-4 HSNM (j)Proposed-4 RSNM (k) Proposed-5 HSNM (l)Proposed-5 RSNM**

**Table 9. SNM improvements**

| Reference no. of SRAM cells | Supply voltage | Technology node | Improvement in SNM Compare with FinFET based 10T SRAM cell using SVL technique at supply =0.9V, Technology node=32nm |
|---|---|---|---|
| [28] | 0.8v | CMOS, 22nm | 18% |
| [38] | 1v | CMOS, 45nm | 2.59% |
| [43] | 0.85v | FinFET, 16nm | 34% |
| [44] | 0.8v | FinFET, 16nm | 13% |

**Table 10. Area overhead analysis for 6T SRAM cell design**

| Compare with conventional SRAM cell Number of transistors =6T | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameters | CMOS SRAM [16] | Proposed-1 | Proposed-2- | Proposed-3 | Proposed-4 | Proposed-5 | CMOS cell using SVL Technique [28] | FinFET cell using SVL Technique [28] |
| Total Number of transistors | 6T | 6T | 8T | 8T | 8T | 8T | 12T | 12T |
| Increment in transistors | None | None | 2T | 2T | 2T | 2T | 6T | 6T |

**Table 11. Area overhead analysis for 10T SRAM cell design**

| Compare with conventional SRAM cell Number of transistor =10T | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Parameters | CMOS SRAM [16] | Proposed-1 | Proposed-2- | Proposed-3 | Proposed-4 | Proposed-5 | CMOS cell using SVL Technique [28] | FinFET cell using SVL Technique [28] |
| Total Number of transistors | 10T | 10T | 12T | 12T | 12T | 12T | 16T | 16T |
| Increment in transistors | 4T | 4T | 6T | 6T | 6T | 6T | 10T | 10T |

### *5.5. Static Power Dissipation*

A device becomes more reliable and faster if its power consumption is reduced. In the CMOS circuit, overall power dissipation arises from static and dynamic power. The reason for static power consumption is leakage current resulting when the circuit is in an OFF condition [41]. Where dynamic power consumption is because of the charging and discharging of capacitors at the output load at a high switching frequency [41]. In the sleep transistor technique, M11 and M12 reduce leakage power. While in the drowsy cache technique, the M12 transistor provides half the supply and helps in reducing the power. In the SVL technique, the LSVL circuit is connected between the ground and the SRAM cell, and the LSVL circuit is not perfectly off due to the PMOS on the state [42]. Therefore, the circuit provides the voltage above the ground level in standby mode, and similarly, the USVL circuit provides a voltage lower than the $V_{DD}$ [42]. In the SVL technique, transistors M11 to M16 helps in reducing leakage power, and this technique gives the best results compared to other. However, the major drawbacks of this technique are that the area increases with the addition of transistors and increases the circuit delay. Therefore, the proposed cell consumes low power using the SVL technique in 32 nm technology and achieves an 80.93% reduction than CMOS -based cells. Tables 7 and 8 illustrate the comparison of static power between cells for 6T and 10T SRAM cells, respectively. Moreover, it can be seen from the tables that as we increase the transistor count in a cell for stability, leakage current and power dissipation are minimized. Static power dissipation in CMOS based 10T and 6T SRAM cells using the SVL technique comes to be 12.5842nw and 15.838nw, while for FinFET based 10T and 6T SRAM cells is 1.0887nw and 1.476nw.

### *5.6. Area Overhead*

For a long time, conventional six transistor cells have been the choice of manufacturers because of reduced area and simplicity in design. From Tables 10 and 11, the proposed cells have an area overhead of a 6T SRAM cell. However, the proposed cells are limited to having a large area, but they can be used where stability and low power are prime concerns. From Table 10, we can say that the area overhead is 2x for the

sleep transistor and drowsy cache techniques, while it is 2.65x for SVL techniques. Similarly, from Table 11, the area overhead is 1.3 x for the first two techniques and 2 x for the SVL technique.

### *5.7. Results and Discussion*

Transistor size is strictly constrained to maintain a cell's data integrity and functionality. Power is wasted a lot in various technologies because any one of the bit lines could discharge with a chance of 1. Therefore, in any write situation, one of the bit lines will discharge its power, resulting in increased power loss. The above cells are making function in the sub-threshold zone to lower the power compensation for those cells. However, 6T SRAM encounters some difficulties in the sub-threshold zone. It has been demonstrated that the cells' inability to write is caused by rising variances and falling signal levels.

From the description above, it is clear that SRAM cells' design complexity and area overhead grow as the number of transistors increases. Therefore, it is necessary to choose a set of transistors that can provide good performance while using less power and having a smaller overall area. When designing SRAM for embedded systems, power consumption is an essential element to consider. Numerous design approaches have been suggested, including the assignment of two threshold voltages ($V_{th}$) and a reduction in supply voltage, which both cut dynamic power and leakage power linearly and quadratically, respectively. Since SRAM consumed a large amount of power to maintain the data, so different techniques were used to minimize the leakage. The combination of supply and transistors arrangement helps in reducing power consumption. All the cells were simulated using HSPICE 2019 and Predictive Technology Model (PTM) models to carry out their ac and dc analysis. With the help of analysis, we can calculate SNM and static power dissipation for all operations. After calculating all values, comparisons are made between different techniques and the technique with the lowest power dissipation value is selected for the design.

## 6. Conclusion

In this paper, novel cells and different parameters that affect the performance of cells are discussed. The paper also includes various leakage power reduction techniques, such as sleep transistors, drowsy caches, and SVL techniques to reduce static power in the cell. Stability and static power are calculated for all the designs at different supply voltages from 200mv to 900mv. It is noticed from the results that all three techniques have some advantages and disadvantages.

From the results, we can say that the drowsy cache is good for static power reduction but has less value of SNM, whereas the sleep transistor has a large value of static power and SNM compared to the drowsy cache technique. Both these techniques have the advantage of reduced areas and delays but are poor performance.

The SVL technique is considered the best for SNM improvement and low leakage power with an area overhead or large delay. Simulation results of 10T SRAM cells are compared with conventional 6T SRAM cells. There is not so much of a large difference in static power for 10T and 6T cells, but a big difference is seen in the SNM of the cells.

There is 37%, 73%, and 19% improvement in HSNM, RSNM, and WSNM, respectively, in 10T SRAM cells compared to conventional 6T cells. There are improvements in SNM by 18% [28], 2.59% [38], 34% [43] and 13% [44] compared to 10T FinFET-based SRAM cells using the SVL technique.

In the future, some other leakage power reduction techniques can be used to design cells for low-power applications.

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