International Journal of Engineering Trends and Technology
ISSN: 2231-5381/ https://doi.org/10.14445/22315381/IJETT-V74I8P105

Volume 74 Issue 8, 68-79, August 2026

Original Article

Simplified Space Vector PWM for a Four-Level NPC Inverter Using a Three-Level SVM Method-Based Carrier-Overlapped PWM Technique

Ong-ard Tubburee[1], Kanyarat Ek-iam[2*]

[1,2]*Department of Industrial Electrical Technology, Faculty of Industrial Technology, Valaya Alongkorn Rajabhat University under the Royal Patronage, Pathum Thani, Thailand.*

[2*]*Corresponding Author : kanyarat@vru.ac.th*

Received: 04 February 2026 Revised: 19 June 2026 Accepted: 24 June 2026 Published: 29 August 2026

Abstract - *In this paper, a simplified Space Vector Pulse-Width Modulation (SVPWM) strategy for a Four-Level Neutral-Point-Clamped (4L-NPC) inverter is proposed on the basis of a Three-Level Space Vector Modulation (3L-SVM) scheme with Carrier-Overlapped PWM (COPWM). The proposed strategy uses only one continuous modulating signal for every phase leg, along with three appropriately positioned triangular carrier waveforms. This method does not require the dwell-time calculation and multi-reference signal generation, unlike classical digital virtual SVPWM and VR-ZSI PWM schemes. The proposed approach restructures 3L-SVM principles into a carrier-based structure and therefore achieves SVM-like voltage utilization and harmonic performance while corresponding to reduced computational complexity. The simulations were conducted in the MATLAB/Simulink environment to validate the proposed strategy and compare it with the PD-PWM and VR-ZSI PWM schemes. The results demonstrated that the proposed COPWM technique enabled stable operation over a wide Modulation index (m_a) range. Moreover, within $0.50 \leq m_a \leq 1.00$, the proposed strategy achieved improved DC-link voltage utilization, thereby improving an average increment of 8.50% and 19.77% in the fundamental line voltage compared to VR-ZSI PWM and PD PWM methods, respectively. In addition, it also provided the lowest Total Harmonic Distortion (THD), reducing phase voltage THD from 67.14% (PD-PWM) and 62.29% (VR-ZSI PWM) to 61.18%. Furthermore, the proposed scheme achieved balanced DC-link capacitor voltages without additional sensing or control strategies. The results demonstrated that the proposed COPWM is a viable compromise between performance and ease of implementation, and it is suitable for real-time control of 4L-NPC inverters.*

Keywords - *4L-NPC, SVPWM, Carrier-Overlapped PWM, 3L-SVM, Modulation index.*

1. Introduction

Multilevel Inverters (MLIs) are considered a key technology in modern power electronic systems and are extensively utilized in medium- to high-power conversion systems, such as renewable energy integration, electric drive systems, and grid-tied converters [1]. As a novel form of inverter, MLIs provide several advantages over the conventional Two-Level Voltage Source Inverters (2L-VSIs) in terms of lower voltage stress on power switches, output voltage quality improvement, Electromagnetic Interference (EMI) reduction, and Total Harmonic Distortion (THD) lowering [2]. Common MLI topologies include Neutral-Point Clamped (NPC) inverters, Flying Capacitor (FC) inverters, Cascaded H-Bridge (CHB) inverters, and Modular Multilevel Converters (MMC) [3, 4]. Among these topologies, the three-level NPC (3L-NPC) inverter is recognized as one of the most suitable configurations for high-power applications, such as rolling mills, pumps, ship propulsion, and wind power generation systems, when the electrical voltage is less than 3-4 kV [5]. Nevertheless, in the past few years, many commercial and industrial applications have required higher power density and efficiency, which has also triggered the evolution of a next generation of multilevel converters or inverters. In this regard, four-level inverters have attracted considerable attention because of their high voltage utilization and better power quality.

The Four-Level Neutral-Point Clamped (4L-NPC) inverter can generate higher voltage levels while eliminating the power switches that are series connected, as depicted in Figure 1, and provides advantages over 2L- and 3L-VSIs, including reduced device voltage rating, improved harmonic performance, higher equivalent switching frequency, and reduced grid-side filter requirements [6]. Nevertheless, the increased number of discrete voltage levels and switching states significantly complicates modulation and control

strategy design, particularly in terms of switching state selection, duty-cycle computation, and real-time implementation.

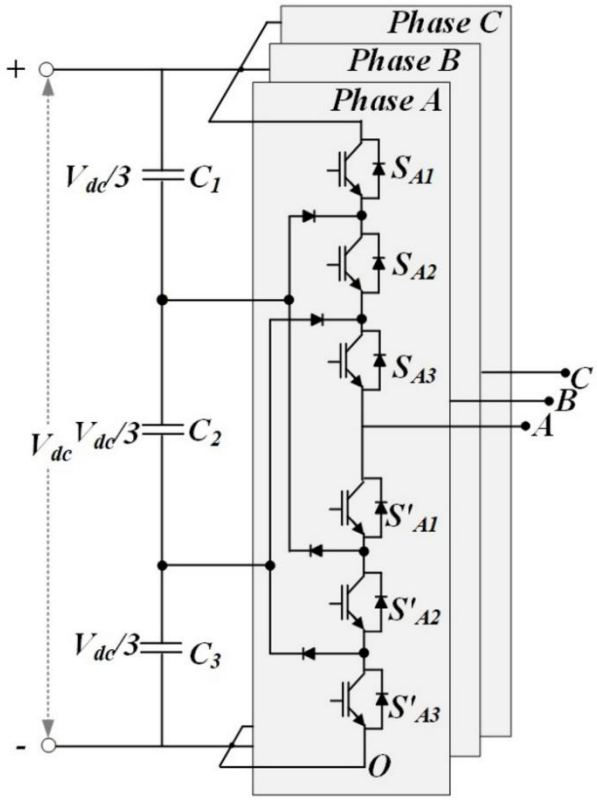

Fig. 1 Circuit architecture of the 4L-NPC inverter

Several modulation strategies are available for 4L-NPC inverters, such as Multi-Carrier Pulse-Width Modulation (MC-PWM), Selective Harmonic Elimination PWM (SHE-PWM), and the Virtual Space Vector PWM (VSVPWM) schemes. Among these schemes, MC-PWM techniques are widely adopted because of their simplicity, low computational burden, and the convenience of implementations by Digital Signal Processors (DSPs). Usually, for the Carrier-Based PWM (CB-PWM) strategy, the switching signals are generated by comparing a reference waveform with several triangular level-shifted or phase-displaced carriers [7, 8]. However, the traditional MC-PWM methods generally suffer from limitations in neutral-point voltage balance and 4L-NPC inverters' output harmonic shaping. SHE-PWM has been extensively studied, where low-order harmonics are eliminated by finding suitable switching angles. However, this technique suffers from a narrow bandwidth response, a limited range of switching angles, and a dependence on costly offline optimization processes [9]. This makes SHE-PWM less effective for wide operating ranges and fast transient response. Alternatively, VSVPWM techniques provide better use of DC-link voltage and lower harmonic distortion, and it also provides a good control strategy to vary the redundant switching states, thus making it suitable for various MLI applications. Incorporating virtual voltage vectors within several switching states enables the VSVPWM to keep the neutral-point currents balanced in one switching period [10]. However, the expansion of the VSVPWM for a four-level inverter (that is, a four-level space vector diagram) results in a large set of complex mathematical expressions with an ample number of virtual space vectors, regions, and sectors. This leads to complexity in calculating the duty cycle and switching sequence, thus making it challenging to be implemented for real-time applications [11].

Numerous modulation techniques have been developed to facilitate the practical functioning of the 4L-NPC inverters. One of the most extensively studied methods involves the utilization of multiple reference signals combined with a zero-sequence injection signal, commonly known as the variable reference with zero-sequence injection PWM (VR-ZSI PWM) method. This method compares synthesized multi-reference waveforms with a single triangular carrier waveform to produce the inverter switching signals during modulation [12, 13]. Although satisfactory performance can be achieved, these methods require the generation and coordination of multiple reference signals, leading to heightened calculation and control complexity. In particular, precise phase synchronization and amplitude normalization are required, which significantly increase implementation difficulty. In response to these drawbacks, effective implementations of CB-PWM with a single reference signal, such as Phase-Disposition PWM (PD-PWM), have been widely researched as a relatively simple approach [14].

Nevertheless, traditional PWM techniques with phase-disposition and level-shifting typically have less flexibility and suboptimal DC-link voltage utilization compared to the SVM scheme. In addition, their effective operation typically requires higher modulation indices. Furthermore, none of these methods can maintain an acceptable switching state at low modulation indices ($m_a < 0.5$) in practice, which restricts their applicability across a wide operating range. This limitation restricts their applicability across a wide operating range. In the literature, Carrier-Overlapped PWM (COPWM) techniques have been introduced to enhance voltage-level utilization and modulation performance, overcoming these limitations [15, 16]. Nevertheless, many reported COPWM and CB-PWM schemes do not explicitly consider neutral-point current dynamics during switching signal generation, thereby increasing the risk of an imbalance in the voltage of the DC-link capacitors. Consequently, to achieve voltage equilibrium across capacitors, supplementary control loops, sensing circuits, or offset-voltage injection methods are typically required to maintain balanced capacitor voltages, thereby increasing the system's complexity, cost, and implementation burden. An unequivocal analysis gap is evident from the preceding discussion. A prevalent modulation strategy for 4L-NPC inverters that maintains the simplicity of CB-PWM implementation is currently absent.

- Maintains simplicity in the implementation of CB-PWM.
- Achieves SVM-level voltage utilization and harmonic performance.
- Operates throughout the modulation index range without necessitating any supplementary balancing control systems.

Motivated by these considerations, this paper proposes a Simpler Space Vector PWM (SVPWM) methodology for a 4L-NPC inverter utilizing a three-level SVM (3L-SVM) method-based COPWM scheme. The proposed method employs a single modulating signal per phase leg in conjunction with three suitably configured triangular carrier waveforms to produce a four-level phase-to-negative DC-link (pole) voltage. By integrating the core principles of 3L-SVM into a CB-PWM framework, the proposed method achieves SVM-like performance with significantly reduced mathematical complexity and implementation burden. This paper's primary contributions can be succinctly summarized as follows:

- Schematic of a simple COPWM based on a single reference signal per phase leg, offering less control complexity than multi-reference signal approaches.
- Enhanced utilization of the DC-link voltage across an extensive modulation index range, facilitating effective inverter operation under various operating conditions.
- Reduced THD at the inverter output side compared to conventional PD-PWM and VR-ZSI PWM methods, as required by loads for improved harmonic performance.
- A user-friendly implementation framework that attains SVM-like performance and is highly suitable for real-time applications.

Therefore, the proposed 3L-SVM method-based COPWM scheme offers a pragmatic and effective solution for high-performance control of a 4L-NPC inverter. The efficacy of the proposed method is verified through comprehensive simulation and comparative analysis by conventional PD-PWM and VR-ZSI PWM schemes.

2. Circuit Configuration and Operating Principle of the 4L-NPC Inverter

2.1. Circuit Configuration of the 4L-NPC Inverter

The circuit configuration of the 4L-NPC inverter is a derivative of the traditional 3L-NPC structure, as illustrated in Figure 1. There are six Controllable Power Switches (CPSs) in each phase leg, which are organized into three complementary switching pairs, which are defined for each leg as $(S_{X1} - S'_{X1})$, $(S_{X2} - S'_{X2})$, and $(S_{X3} - S'_{X3})$, where $X \in \{A, B, C\}$ refers to the index of the three-phase grid system. In each pair, the upper and lower CPSs operate complementarily to prevent DC-link shoot-through.

In addition, the CPSs are interfaced to clamping diodes connecting the output node of each phase leg and the corresponding intermediate DC-link nodes for multilevel voltage synthesis. Under balanced DC-link conditions, the input voltage is partitioned by three series-connected capacitors (C_1, C_2, and C_3) so that the total DC-link voltage has equal distribution, each maintaining a voltage of $V_{dc}/3$. Consequently, the blocking voltage across individual CPS is limited to a fraction of the input voltage. When compared with the traditional 2L-VSIs and 3L-VSIs, the device voltage stress of the 4L-NPC topology is considerably reduced without series-connected switches. Therefore, the 4L-NPC inverter has better voltage utilization and output voltage quality, providing it appropriate for medium- and high-power applications.

2.2. Operating Principle and Voltage Level Generation

According to the inverter topology and the possible switching conditions of CPSs in the three-phase leg of the proposed inverter, the switching equation (S_X) for phase X is expressed as:

$$S_X = \sum_{i-1}^{3} S_{Xi} = S_{X1} + S_{X2} + S_{X3} \quad (1)$$

Where $S_{Xi} \in \{0, 1\}$ denotes the switching state of the i-th CPS in phase X, with logic "1" and "0" representing the ON and OFF states, respectively. To ensure valid operating states and safe commutation, the following constraint must be satisfied:

$$0 \leq S_{X1} \leq S_{X2} \leq S_{X3} \leq 1$$

Assuming balanced conditions for the DC-link capacitor voltages, the total DC-link voltage is properly shared across the three series-connected capacitors, with each capacitor maintaining a voltage of $V_{dc}/3$. According to the circuit configuration, the instantaneous pole voltage is expressed as

$$V_{XO} = \frac{V_{dc}}{3}(S_{X1} + S_{X2} + S_{X3}) \quad (2)$$

Equation (2) shows that each phase leg of the 4L-NPC inverter is capable of synthesizing four discrete voltage levels, namely 0, $V_{dc}/3$, $2V_{dc}/3$, and V_{dc}, depending on the selected switching states. The correlation between switching conditions and the associated pole-voltage levels is detailed in Table 1.

Table 1. Switching states and pole-voltage levels of the 4L-NPC inverter

Voltage Level	S_{X1}	S_{X2}	S_{X3}	S'_{X1}	S'_{X2}	S'_{X3}	V_{XO}
0	0	0	0	1	1	1	0
1	0	0	1	1	1	0	$V_{dc}/3$
2	0	1	1	1	0	0	$2V_{dc}/3$
3	1	1	1	0	0	0	V_{dc}

According to Table 1, the following Operating Rules (ORs) of the 4L-NPC inverter can be derived:

- For each phase leg, the CSPs operate mutually exclusively in a manner where the upper and lower devices are not simultaneously activated. This avoids DC-link shoot-through, leading to assured operation safety.
- The switching sequence must satisfy the hierarchical constraint such that S_{x3} is turned ON before S_{x2}, and S_{x2} is turned ON before S_{x1}, ensuring proper voltage level generation and safe commutation.

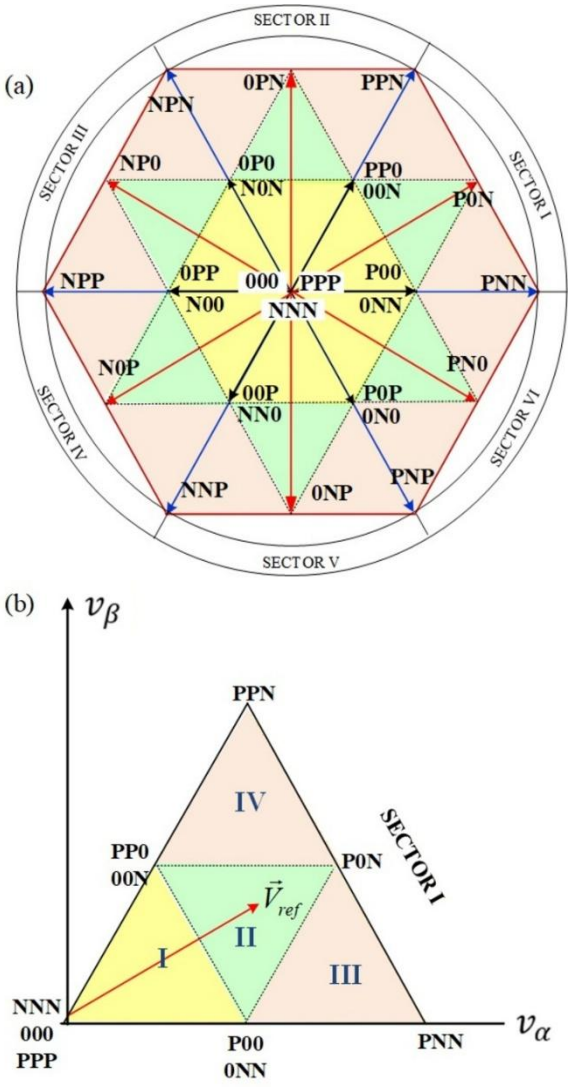

Fig. 2 Space vector diagram of the 3L-SVM, (a) Complete space vector diagram, and (b) Region II in sector I.

3. Modulation Signal Generation Based on 3L-SVM Scheme

The SVM scheme is a digital modulation strategy that produces the switch driving signals with respect to the vector representation of the original inverter switching states presented in a stationary α-β reference frame. The discrete inverter switching states in the SVM scheme are mapped to voltage vectors of fixed amplitudes and angles, with switching signals applied directly to the CPSs based on the given sequence of selected vectors. The SVM diagram for a three-level inverter is hexagonally shaped and consists of several concentric regions (as shown in Figure 2(a)). This strategy has 27 potential switching states, which correspond to 19 different voltage vectors in the α-β plane. These vectors are symmetrically divided into four groups according to their magnitude: the zero vector, $\vec{V}_0$; small vectors, $\vec{V}_1 - \vec{V}_6$; medium vectors, $\vec{V}_7 - \vec{V}_{12}$; and large vectors, $\vec{V}_{13} - \vec{V}_{18}$. Redundancy occurs in some vector groups, since several switching states yield the same voltage vector. That is, three redundant switching states correspond to the zero vector and two equivalent switching states associated with each small vector. By comparison, the medium and large vectors cannot be expressed with dual switching configurations; they are uniquely defined, non-redundant representations.

3.1. Dwell Time Calculation

The fundamental concept of the 3L-SVM technique relies on the identification of the Nearest Three Vectors (NTVs) to generate the reference voltage vector ($\vec{V}_{ref}$). Within each sampling period (T_S), the instantaneous value of the $\vec{V}_{ref}$ is generated by a time-weighted combination of the NTVs associated with the corresponding triangular region, where each vector is applied for a specific dwell time. This ensures volt-second balance over the switching interval. For instance, when the $\vec{V}_{ref}$ is positioned in sector I within region II, as illustrated in Figure 2(b). It is constructed using the adjacent voltage vectors $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_7$. Accordingly, the volt-second balance expression is:

$$\vec{V}_{ref}T_S = 2\left[t_1\vec{V}_1 + t_7\vec{V}_7 + t_2\vec{V}_2\right] \tag{3}$$

Where t_1, t_2, and t_7 denote the dwell times associated with vectors $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_7$, respectively. Equation (3) can be deconstructed into its α-β components within the stationary reference frame as

$$\begin{cases} V_{ref}cos\theta = \frac{2V_{dc}}{\sqrt{3}T_S}\left(\frac{1}{\sqrt{3}}t_1 + \frac{1}{\sqrt{3}}t_2 cos\frac{\pi}{3} + t_7 cos\frac{\pi}{6}\right) \\ V_{ref}sin\theta = \frac{2V_{dc}}{\sqrt{3}T_S}\left(\frac{1}{\sqrt{3}}t_2 sin\frac{\pi}{3} + t_7 sin\frac{\pi}{6}\right) \end{cases} \tag{4}$$

Where θ is the phase angle of the $\vec{V}_{ref}$. By solving (4), the dwell time expressions for t_1, t_2, and t_7 are obtained as

$$\begin{cases} t_1 = \frac{1}{2}(T_S - 2m_a T_S \sin\theta) \\ t_2 = \frac{1}{2}\left(T_S - \sqrt{3}m_a T_S \cos\theta + m_a T_S \sin\theta\right) \\ t_7 = \frac{1}{2}(-T_S + \sqrt{3}m_a T_S \cos\theta + m_a T_S \sin\theta) \end{cases} \tag{5}$$

Where m_a denotes the modulation index. In an MLI operating under the SVM scheme, the modulation index is commonly defined as the normalized magnitude of the $\vec{V}_{ref}$ relative to the total DC-link voltage (V_{dc}):

$$m_a = \frac{\sqrt{3}V_{ref}}{V_{dc}} \tag{6}$$

When the $\vec{V}_{ref}$ moves across other triangular regions and sectors, the corresponding dwell time equations are derived using the same analytical procedure, by selecting the appropriate set of NTVs and applying the same vector decomposition and projection principles.

3.2. Symmetrical Switching Sequence Design

In the literature, switching sequence designs adopting the SVM method are generally divided into two primary types: continuous switching sequence designs and discontinuous switching sequence designs. Discontinuous switching sequences are widely adopted in many inverter applications due to their capability to reduce switching losses by clamping one or more CPSs during a portion of the fundamental period. But the CPSs always operate with discontinuous switches, which usually result in higher THD and Common-Mode Voltage (CMV). These limitations are fundamentally due to the asymmetrical neutral point current flow and the imbalanced DC-link voltage issue [17]. To suppress the negative impact of discontinuous commutation, a continuous switching sequence design has been introduced, where at each sampling instant, it is attempted to equally switch all fundamental CPSs. Continuous switching patterns can produce higher-quality output voltage, lower THD, and lower CMV due to an even flow of the neutral-point current distribution as well as symmetrical voltage transition [18]. However, such scenarios result in increased switching losses inherently owing to a great number of switching commutations. A symmetrical switching-sequence design is employed to mitigate switching losses while preserving the advantages of continuous modulation by symmetrically arranging the switching states within each sampling interval. Figure 3 illustrates an example of the symmetrical switching sequence of sector I within region II.

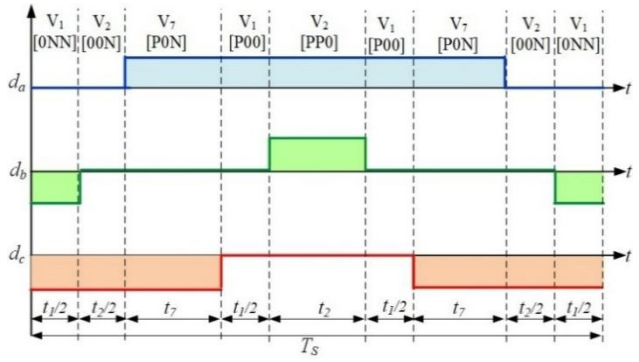

Fig. 3 Symmetrical switching sequence design and dwell time in sector I within region II

3.3. Three-Phase Modulating Signal Generation

As depicted in Figure 3, the switching states of the NTVs associated with the voltage vectors are employed to synthesize the $\vec{V}_{ref}$. For the case under consideration, vector $\vec{V}_1$ is used for redundant switching states P00 and 0NN, and $\vec{V}_2$ for PP0 and 00N, whereas $\vec{V}_7$ utilizes vector P0N following a symmetric sequence of switching patterns. The conduction times of the CPSs in each phase leg, T_A, T_B, and T_C, are determined depending on the driving pattern as follows:

$$\begin{cases} T_A = \frac{2}{T_S}\left(\frac{t_1}{2} + \frac{t_2}{2} + t_7\right) \\ T_B = \frac{2}{T_S}\left(-\frac{t_1}{2} - \frac{t_2}{2}\right) \\ T_C = \frac{2}{T_S}\left(-\frac{t_1}{2} - \frac{t_2}{2} + t_7\right) \end{cases} \tag{7}$$

The three-phase continuous modulation signals are generated by projecting the selected voltage vectors onto the stationary α-β reference frame and scaling the conduction intervals of the three-phase leg with respect to the switching period (T_S). Thus, for region II of sector I, the modulation signal equations become expressed as

$$\begin{cases} v_{mA} = \frac{\sqrt{3}}{2}m_\alpha + \frac{1}{2}m_\beta \\ v_{mB} = -\frac{\sqrt{3}}{2}m_\alpha + \frac{3}{2}m_\beta \\ v_{mC} = -\frac{\sqrt{3}}{2}m_\alpha - \frac{1}{2}m_\beta \end{cases} \tag{8}$$

Where $m_\alpha = m_a cos\theta$ and $m_\beta = m_a sin\theta$, with m_a denoting the modulation index, which varies within the modulating range of 0 to 1. The same analytical procedure is applied to all sectors and regions of the three-level space vector diagram. The mathematical expressions for the three-phase continuous modulation signals corresponding to each sector are shown in Table 2.

Table 2. Three-phase modulation signal expressions for six sectors

Sectors	Modulation signal expressions
I & IV	$v_{mA} = \sqrt{3}/2m_\alpha + 1/2m_\beta$ $v_{mB} = -\sqrt{3}/2m_\alpha + 3/2m_\beta$ $v_{mC} = -\sqrt{3}/2m_\alpha - 1/2m_\beta$
II & V	$v_{mA} = \sqrt{3}m_\alpha$ $v_{mB} = \sqrt{3}m_\beta$ $v_{mC} = -\sqrt{3}m_\beta$
III & VI	$v_{mA} = \sqrt{3}/2m_\alpha - 1/2m_\beta$ $v_{mB} = -\sqrt{3}/2m_\alpha + 1/2m_\beta$ $v_{mC} = -\sqrt{3}/2m_\alpha - 3/2m_\beta$

Referring to Table 2, the modulation signal equations of sectors I and IV, II and V, and III and VI are the same, respectively, although the dwell time derivations for individual regions and sectors are given by different voltage vector combinations. Consequently, the same modulation

formulation can be reused for each pair of sectors, which significantly reduces computational complexity and facilitates efficient real-time digital implementation.

4. Proposed COPWM Technique

In comparison with the conventional SVPWM scheme, the CB-PWM techniques offer a simpler and more intuitive implementation, particularly for MLI applications. In this research, a COPWM scheme is proposed to achieve SVM-like voltage utilization and harmonic performance while preserving the simplicity of a carrier-based approach.

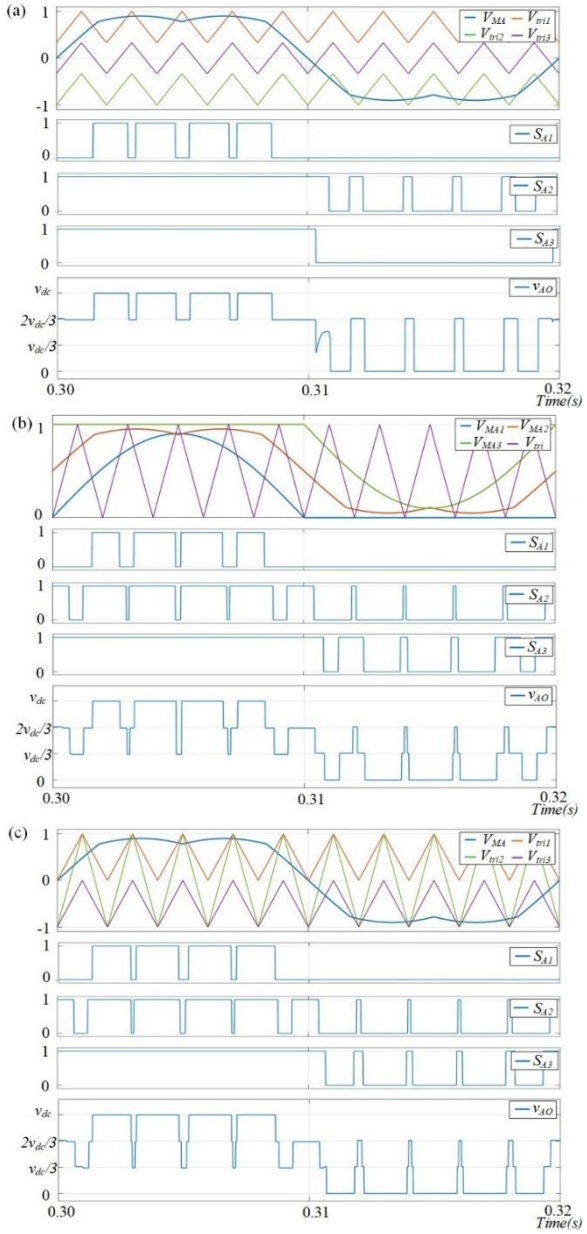

Fig. 4 Comparison of different PWM schemes showing the a-phase modulating signal and corresponding three-phase switch driving signals (f_{sw} = 500 Hz, m_a = 0.9), (a) Conventional PD-PWM, (b) VR-ZSI PWM, and (c) Proposed COPWM.

As illustrated in Figure 4(c), the proposed COPWM technique employs three triangular carrier signals, denoted as v_{tri1}, v_{tri2}, and v_{tri3}, organized also as a hybrid and phase-locked configuration. The triangular carrier signals v_{tri1} and v_{tri3} have a normalized magnitude of unity, with operating ranges of 0 to 1 and 0 to −1, respectively, and are arranged according to the Level-Shifted Carrier (LSC) PWM technique. In contrast, the carrier signal v_{tri2} has a magnitude of 2, spanning the range from −1 to 1, and is positioned such that its positive and negative peak amplitudes coincide with the upper and lower extrema of v_{tri1} and v_{tri3}, respectively. For each phase leg, the three triangular carrier signals are compared with a single continuous modulating waveform derived from the 3L-SVM principle, which eliminates the need for multiple reference signals and complex dwell-time calculations.

4.1. Switch Driving Signal Generation and Operating Rule Compliance

The switch driving signals of the CPS in each phase leg are generated directly with a comparator-based approach between the three-phase continuous modulating signal, which is obtained through the 3L-SVM scheme (as illustrated in Table 2), and three triangular carrier signals, which are derived through the COPWM technique. This method provides a simple implementation approach, but keeps all the properties of SVM in place. In particular, for a single-phase leg, the switching states of the upper CPSs, when compared to the modulating signal with each of the carrier signals v_{tri1}, v_{tri2}, and v_{tri3}, are:

$$\begin{cases} S_{X1} = 1, \ v_{mX} \geq v_{tri1} \\ S_{X2} = 1, \ v_{mX} \geq v_{tri2} \\ S_{X3} = 1, \ v_{mX} \geq v_{tri3} \end{cases} \tag{9}$$

The proposed method assigns complementary switch driving signals to the corresponding lower CPSs for safe operation and to avoid a DC-link shoot-through situation. Then, based on the resulting switching patterns of all complementary switch pairs, it is confirmed that the proposed COPWM technique strictly satisfies the ORs of the 4L-NPC inverter. Specifically, a pair of complementary switches takes effect in a mutually exclusive way, thus avoiding a DC-link short circuit. In addition, the hierarchical switching constraint is retained in that S_{X3} must be activated before S_{X2}, and S_{X2} should be preceded by the activation of S_{X1}. The organized and chained switching mechanism generates the proper voltage steps and enables safe transitions between switching states. This approach makes the pole voltage synthesized from a series of transitions amongst four discrete voltage states: 0, $V_{dc}/3$, $2V_{dc}/3$, and V_{dc}. This structured voltage synthesis inherently satisfies the physical constraints imposed by the 4L-NPC circuit configuration while providing a consistent framework for generating high-quality output waveforms. Therefore, it assists in ensuring the inverter output has both high quality and lower harmonic distortion.

4.2. Voltage Level Synthesis and DC-Link Utilization

The main benefit of the proposed COPWM technique is its improved utilization of input voltage via synchronized switching actions and systematic approaches to voltage level synthesis. In the conventional PD-PWM method, as shown in Figure 4(a), the independent comparison between a single reference signal and multiple triangular carrier signals often leads to incomplete voltage transitions and underutilization of available voltage levels. Similarly, in the VR-ZSI PWM scheme, as illustrated in Figure 4(b), although zero-sequence injection can partially enhance voltage utilization, the presence of multiple reference signals may result in non-uniform intersections with a single triangular carrier signal, thereby limiting effective voltage synthesis. In contrast, the proposed COPWM technique employs a single SVM-derived modulating signal that inherently satisfies the volt-second balance condition. The average pole voltage over one switching period (T_S) is expressed as

$$\overline{v_{XO}} = \frac{1}{T_S}\int_0^{T_S} v_{XO}(t)\,dt \tag{10}$$

For a 4L-NPC inverter, the instantaneous pole voltage is determined by the switching states, as given in Equation (2), where $S_{X1}, S_{X2}, S_{X3} \in \{0, 1\}$ represents the switching functions of the upper switching devices. Substituting into Equation (10), the averaged pole voltage is expressed as

$$\overline{v_{XO}} = \frac{V_{dc}}{3}(D_{X1} + D_{X2} + D_{X3}) \tag{11}$$

where D_{X1}, D_{X2}, and D_{X3} denote the duty cycles of the corresponding switching states within one switching period. In the conventional PD-PWM method, due to the lack of coordination among switching signals, the duty cycles associated with higher voltage levels are often reduced or discontinuous, thereby resulting in suboptimal utilization of the input voltage. In the VR-ZSI PWM scheme, although voltage utilization can be improved through zero-sequence injection, the use of multiple reference signals introduces non-uniform duty cycle distribution. Meanwhile, the proposed COPWM technique guarantees coordinated duty cycles D_{X1}, D_{X2}, and $D_{X3,}$ in an orderly and consecutive manner using the hierarchical switching constraint.

$$S_{X3} \rightarrow S_{X2} \rightarrow S_{X1}$$

This coordinated activation ensures that higher voltage levels are engaged and held progressively for longer periods of time, so as to maximize the contribution of high-level switching states to the averaged output voltage. Therefore, the fundamental voltage component of the output voltage is expressed as

$$V_1 \approx m_a \frac{V_{dc}}{2} \tag{12}$$

This effect enhances the output voltage because the charge creates a more prolonged and stable hold at elevated voltage levels. Consequently, the pole voltage (v_{XO}) exhibits longer high-level switching intervals, thereby improving DC-link voltage utilization and increasing the fundamental output voltage component.

4.3. Harmonic Performance and THD Reduction

The spectrum of the output voltage provides valuable insights when assessing the harmonic performance of PWM inverters. As a result, the pole voltage is represented as:

$$v_{XO}(t) = V_1 sin(\omega t) + \sum_{n=2}^{\infty} V_n sin(n\omega t + \phi_n) \tag{13}$$

Where V_1 and V_n are the fundamental voltage and harmonic voltage components, respectively. Thus, the output voltage THD is defined as

$$THD = \sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{V_1}\right)^2} \tag{14}$$

In general, THD of the output voltage is typically dominated by low-order harmonics, which are substantially impacted by the switching instant distribution. The low-frequency harmonic components are increased due to the fact that irregular switching intervals and abrupt voltage transitions inject a large number of harmonics into the circuit, while uniformly distributed switching events push this harmonic energy toward higher frequencies. Thus, the conventional PD-PWM method is more likely to have higher THD (uncontrolled switching with narrower pulses), and the VR-ZSI PWM scheme may lead to unequal switching intervals because of the reference signal alteration. In contrast, the proposed COPWM technique ensures a uniform and symmetrical distribution of switching patterns obtained through the COPWM structure. This results in smoother voltage transitions and reduced discontinuities, which can be interpreted as a reduction in dv_{XO}/dt. In addition, the SVM-based modulating signal satisfies the volt-second balance condition.

$$\int_0^{T_S} v_{XO}(t)\,dt = V_1 T_S \tag{15}$$

There by minimizing the low-frequency component. Consequently, the pole voltage exhibits a smoother staircase waveform, and the line voltage benefits from increased effective voltage levels. This leads to a reduction in low-order harmonics and, hence, a lower THD compared to the conventional PD-PWM and the VR-ZSI PWM schemes.

4.4. Implementation Simplicity and Hardware Feasibility

The proposed COPWM scheme preserves the simplicity of conventional CB-PWM while achieving SVM-like performance. In real-time implementation, the computational burden mainly consists of carrier generation, comparison with

a single modulating signal, and direct switching-state generation. This method is different from the traditional SVPWM approaches, as it does not require sector identification or dwell time calculation, which can lower the computation burden. In particular, the three triangular carrier signals are generated by conventional triangular waveform generators (properly scaled), and the modulating signal is derived once per sampling period. Its switching functions are generated using three parallel comparators and basic logical operations. The proposed method does not require additional sensing variables, predictive control algorithms, or online recalculation processes. In terms of implementation, the proposed COPWM technique is highly compatible with both DSP and FPGA platforms. For DSP-based systems, it can be implemented on standard PWM modules with atomic processing overhead, allowing for efficient real-time control of the system's output signals. In FPGA implementation, the carriers can be generated using counters, while the modulating signal can be obtained via LUT or CORDIC-based methods, thereby improving low logic resource utilization.

At this stage, the validation is limited to analytical and simulation-based evaluation to isolate the intrinsic effects of the proposed modulation strategy from hardware-dependent factors, such as parasitic, noise, and switching delays, ensuring a fair comparison among the PD-PWM, VR-ZSI PWM, and the COPWM schemes. Despite the absence of experimental results, the proposed method is fully compatible with practical hardware implementation and does not require additional devices or auxiliary circuits beyond conventional MLI structures. Therefore, the proposed COPWM technique offers a favorable trade-off between performance improvement and can be considered hardware-feasible with low computational burden.

5. Results and Discussions

The developed simplified SVPWM scheme for a 4L-NPC inverter based on the 3L-SVM method-based COPWM algorithm was validated by detailed simulations carried out in MATLAB/Simulink. To a fair comparison could be made, the proposed method was benchmarked against a conventional PD-PWM and VR-ZSI PWM schemes with the same operating and control conditions. The key system parameters used for simulation are summarized in Table 3.

Table 3. Key parameters of the simulation system

Parameters	Symbols	Value
Total DC-link voltage	V_{dc}	100 V
Input capacitors	C_1, C_2 and C_3	2200 µF
Output resistance	R_o	50 Ω
Output inductance	L_o	25 mH
Carrier frequency	f_{car}	5 kHz
Line frequency	f_L	50 Hz

5.1. Steady-State Performance Comparison

The steady-state simulation results of the 4L-NPC inverter operating under the conventional PD-PWM, VR-ZSI PWM, and the proposed COPWM schemes are illustrated in Figure 5-7, respectively, at a modulation index of m_a = 0.90. The comparison focused on output voltage waveform quality, fundamental voltage magnitude, and THD of output voltage.

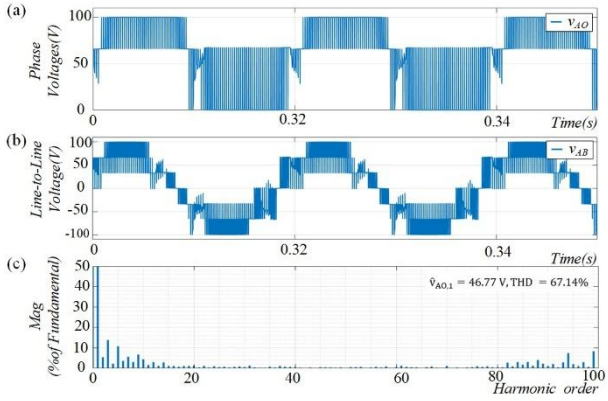

Fig. 5 Steady-state simulated results of the 4L-NPC inverter operating under the PD-PWM scheme at m_a = 0.90. (a) Pole voltage, (b) Line voltage, and (c) Pole voltage THD.

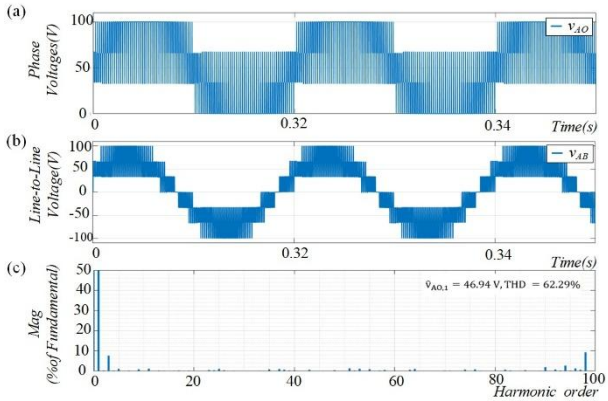

Fig. 6 Steady-state simulated results of the 4L-NPC inverter operating under the VR-ZSI PWM scheme at m_a = 0.90. (a) Pole voltage, (b) Line voltage, and (c) Pole voltage THD.

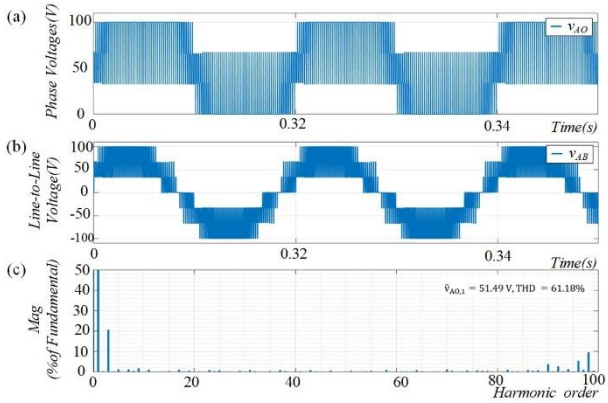

Fig. 7 Steady-state simulated results of the 4L-NPC inverter operating under the proposed COPWM scheme at m_a = 0.90. (a) Pole voltage, (b) Line voltage, and (c) Pole voltage THD.

For all three PWM schemes, the simulated waveforms are consistent with the operating principle of the 4L-NPC inverter. As observed in Figure 5(a)-7(a), the pole voltage (v_{AO}) exhibited a typical four-level staircase waveform, consisting of discrete voltage levels of 0 V, 33.33 V, 66.67 V, and 100 V, corresponding to 0, V_{dc}/3, 2V_{dc}/3, and V_{dc}, respectively. This confirmed that all modulation strategies satisfied the switching constraints and correctly synthesized the four-level output voltage. Similarly, the line-voltage (v_{AB}), shown in Figure 5(b)-7(b) presented a higher number of voltage steps (seven steps) in comparison to the phase voltage. This multi-level composition resulted from the phase-to-phase voltage difference and resulted in smoother output waveforms because harmonic components partially canceled each other. However, in spite of this common structural behavior, the quality of the output waveform is much different among the three PWM methods. In Figure 5, the conventional PD-PWM scheme generated intermittent switching timings and non-uniform voltage transitions that can produce a distorted staircase waveform. The a-pole voltage harmonic spectrum in Figure 5(c) indicated that the voltage THD rises to a high value of 67.14%, which was mainly caused by the existence of low-order harmonics.

The simulated waveforms of the VR-ZSI PWM scheme (Figure 6) improved the regularity of switching transitions, thereby stabilizing the staircase waveform across channels. Consequently, the voltage THD decreased from 67.14% to 62.29%. However, the introduction of multiple reference signals introduced a small asymmetry in switching intervals, which limits further harmonic reduction. In contrast, the proposed COPWM technique, as shown in Figure 7, exhibited the most stable and uniform switching characteristics. The a-pole voltage waveform showed distinctive and evenly distributed voltage steps, indicating that the switching patterns are coordinated properly. This further reduced the voltage THD to 61.18%, which is the lowest among all three methods. Additionally, the fundamental voltage component is 46.77 V for the PD-PWM method and 46.94 V for the VR-ZSI PWM scheme, compared to 51.49 V for the proposed COPWM technique. This improvement could be attributed to better performance in DC-link voltage utilization; specifically, that higher-voltage states are involved for longer periods within each switching cycle. Overall, the results confirmed that while all three PWM schemes correctly realize the four-level pole voltage and seven-level line voltage waveforms of the 4L-NPC inverter, the proposed COPWM technique provided superior steady-state performance regarding waveform quality, harmonic reduction, and voltage utilization.

5.2. Dynamic and Comparative Performance Evaluation

Figure 8-11 illustrate the dynamic and comparative performance of the 4L-NPC inverter operating under the PD-PWM, VR-ZSI PWM, and the proposed COPWM schemes, respectively, when the modulation index is varied continuously over the wide modulating range (0.0 to 1.0). The comparison focused on the transient behavior of the line voltage (v_{AB}), three-phase currents (i_A, i_B, and i_C) at the output side, and three capacitor voltages (v_{C1}, v_{C2}, and v_{C3}) at the input side.

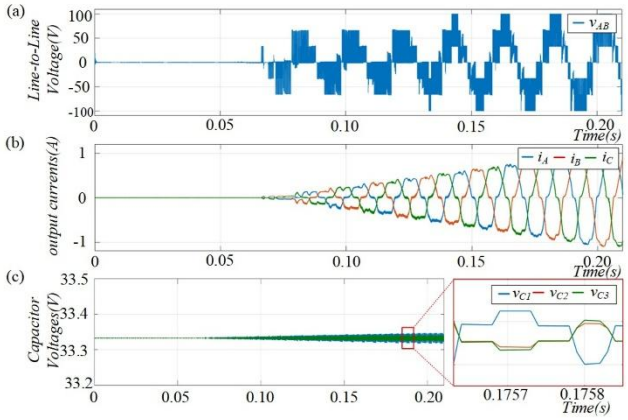

Fig. 8 Dynamic responses of the 4L-NPC inverter operating under the PD-PWM scheme over a wide modulation range ($0 < m_a \leq 1$), (a) Line voltage, (b) Output phase currents, and (c) Split capacitor voltages.

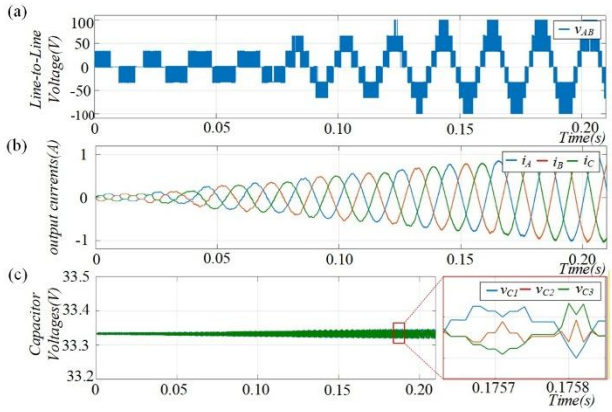

Fig. 9 Dynamic responses of the 4L-NPC inverter operating under the VR-ZSI PWM scheme over a wide modulation range ($0 < m_a \leq 1$), (a) Line voltage, (b) Output phase currents, and (c) Split capacitor voltages.

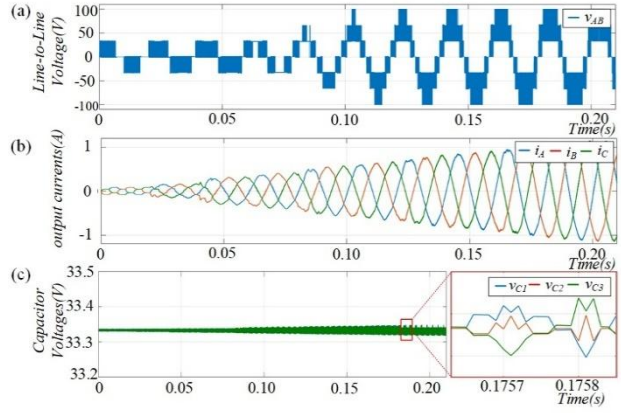

Fig. 10 Dynamic responses of the 4L-NPC inverter operating under the proposed COPWM scheme over a wide modulation range ($0 < m_a \leq 1$). (a) Line voltage, (b) Output phase currents, and (c) Split capacitor voltages.

As shown in Figure 8, the conventional PD-PWM scheme exhibited limited dynamic capability, particularly in the low modulation range. In this duration, the comparison between the single reference waveform and the three triangular carrier waves failed to generate valid switching states that satisfy the ORs of the 4L-NPC inverter. As a result, proper voltage level synthesis could not be maintained, leading to distorted line voltage waveforms and delayed output current response. As the modulation index increases, the line voltage (v_{AB}) gradually transitioned from lower-level operation to a full seven-level waveform when m_a > 0.66. However, this transition occurs later compared to other methods, suggesting a later completion of higher voltage levels. Moreover, significant voltage ripples and imbalance can be seen in the voltages across the DC-link capacitors during dynamic transients, as illustrated by higher variations of these voltages.

In Figure 9(a), the dynamic behavior of the VR-ZSI PWM scheme outperformed that of the conventional PD-PWM method. The line voltage waveform transitions in a less severe (smoother) manner, and output currents exhibited better sinusoidal indices (better shape) during modulation index variation. Half of the full seven-level waveform for the line voltage could be formed at lower modulation indices (m_a > 0.61), suggesting more effective voltage level activation than the PD-PWM method.

Moreover, the DC-link capacitor voltages remained close to $V_{dc}/3$ with little variation under all operational conditions, thereby demonstrating robust neutral-point voltage control. In contrast, the proposed COPWM technique, as illustrated in Figure 10, achieves the highest levels of consistent and dynamic performance in a single manner. With m_a > 0.51, the line voltage (v_{AB}) achieved a full seven-level waveform at a modulation index that is lower than typical thresholds, leading to better utilization as higher voltage levels are activated earlier.

The voltage waveform had smooth and well-defined transitions throughout the entire modulation range. It generated balanced, sinusoidal output currents with fast dynamic response and low distortion. In addition, the proposed COPWM technique maintained very stable and well-balanced DC-link capacitor voltages around $V_{dc}/3$, similar to the VR-ZSI PWM scheme. However, from an implementation point of view, the proposed COPWM technique is particularly advantageous.

This modulation strategy employed a single reference signal per phase leg derived from SVM and uses three triangular carrier signals with a simplified, more direct control structure. Conversely, the VR-ZSI PWM scheme needs several reference signals as additional inputs with different waveform characteristics, which makes it more complex and computationally intensive during the design process.

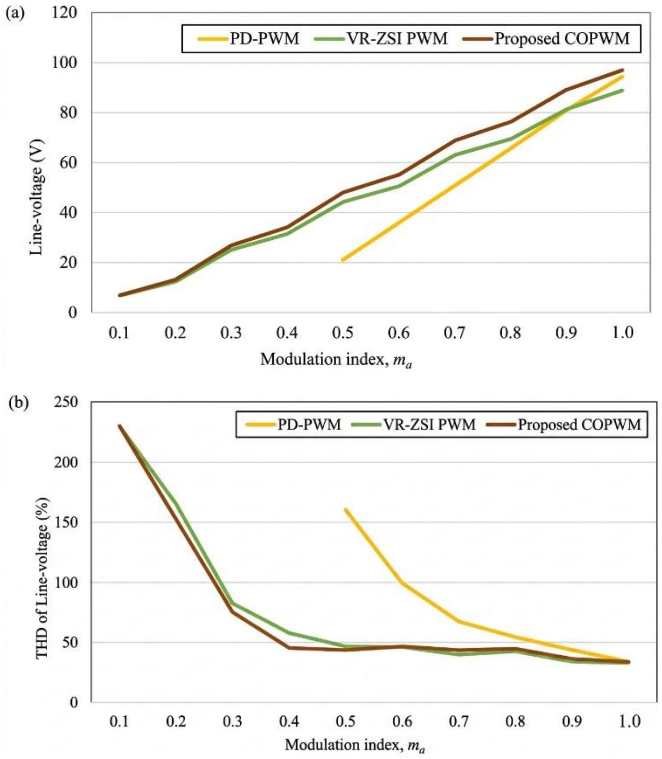

Fig. 11 Summary comparison of the 4L-NPC inverter performance under the three PWM schemes over a wide modulation index range, (a) Fundamental voltage component of the line voltage, and (b) Line voltage THD.

Figure 11 summarizes the comparative performance of the three PWM schemes over a wide modulation index range, serving as a quantitative confirmation of the dynamic behaviors observed in Figure 8-10. It was observed that the conventional PD-PWM scheme operated effectively only for m_a > 0.50. For m_a < 0.50, valid switch driving signals could not be generated to satisfy the operating ORs of the 4L-NPC inverter, which is consistent with the distorted dynamic waveforms and delayed voltage level formation observed in Figure 8. As shown in Figure 11(a), the proposed COPWM technique achieved the highest fundamental voltage component of the line-voltage across the entire modulation range, indicating superior input voltage utilization. This behavior is consistent with the earlier formation of the seven-level voltage waveform at lower modulation indices (m_a > 0.51) observed in Figure 10, compared to the VR-ZSI PWM scheme (m_a > 0.61) and the conventional PD-PWM method (m_a > 0.66). A quantitative comparison in the range 0.50 ≤ m_a ≤ 1.00 shows that the proposed COPWM technique achieved an average line voltage that is 8.50% higher than the VR-ZSI PWM scheme and 19.77% higher than the PD-PWM method, confirming its improved DC-link voltage utilization. Figure 11(b) further showed that the line-voltage THD decreased with increasing modulation index for all methods. The proposed COPWM technique consistently achieved the lowest voltage THD, particularly in the medium-to-high modulation region. This confirmed that the superior steady-state

performance of the proposed COPWM technique originates from its improved dynamic voltage level activation capability.

6. Conclusion

This paper proposes a simplified SVPWM strategy for a Four-Level Neutral-Point-Clamped (4L-NPC) inverter using a three-level SVM-integrated Carrier-Overlapped PWM (COPWM) strategy. The proposed approach employs a single SVM-based modulating signal for each phase leg together with three coordinated triangular carrier signals, thereby simplifying switching-signal generation without requiring sector identification or dwell-time calculation. Consequently, the proposed method significantly reduces computational complexity while maintaining SVM-like performance. The steady-state, dynamic, and comparative simulation results demonstrate that the proposed COPWM technique provides superior input-voltage utilization, harmonic performance, and operating capability compared with the conventional PD-PWM and VR-ZSI PWM methods. Particularly, the proposed approach provides a fundamental line voltage that is, on average, 8.50% higher than that of the VR-ZSI PWM scheme and 19.77% larger than the conventional PD-PWM method, leading to better DC-link utilization. Furthermore, the proposed scheme consistently provides lower voltage THD because of its symmetrical and uniformly distributed switching patterns. From a dynamic performance perspective, the presented COPWM strategy enables earlier activation of complete seven-level voltage synthesis at lower modulation indices, providing an enhanced transient response and a larger feasible operating region.

Additionally, the proposed method achieves natural DC-link capacitor voltage balancing without requiring additional neutral-point current sensing or offset-voltage injection techniques. By using a single reference signal per phase leg instead of multiple reference waveforms, the proposed COPWM technique achieves a considerably simpler control structure with reduced implementation complexity compared to the VR-ZSI PWM scheme while achieving similar voltage balancing performance.

In summary, the proposed 3L-SVM-based COPWM scheme has demonstrated high performance, wide operating capability, and low implementation complexity for 4L-NPC inverter applications. These characteristics make it well-suited for real-time digital control and industrial applications of multilevel power converters. Future work will focus on experimental validation to further verify the proposed 3L-SVM-based COPWM strategy under practical operating conditions.

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgment

The authors would like to express their sincere gratitude to the faculty of industrial technology and the research and development institute of Valaya Alongkorn Rajabhat University under the Royal Patronage for their continuous support and research funding that made this work possible.

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