International Journal of Engineering Trends and Technology
ISSN: 2231-5381/ https://doi.org/10.14445/22315381/IJETT-V74I8P135

Volume 74 Issue 8, 518-534, August 2026

Original Article

Implementation of Asymmetrical Cascaded H-Bridge Multilevel Inverter with Flyback Converter for Solar Photovoltaic System

C Dinakaran[1], T Padmavathi[2]

[1]*Department of Electrical and Electronics Engineering, GITAM School of Core Engineering, GITAM (Deemed to be University), Visakhapatnam, Andhra Pradesh, India,*
[2]*Department of Electrical, Electronics and Communication Engineering, GITAM School of Core Engineering, GITAM (Deemed to be University), Visakhapatnam, Andhra Pradesh, India.*

[1]*Corresponding Author : dina4karan@gmail.com*

Received: 16 September 2025 Revised: 24 July 2026 Accepted: 29 July 2026 Published: 29 August 2026

Abstract - *The growing interest in multilevel inverters for high-power applications is largely attributable to their ability to lower Total Harmonic Distortion (THD) in the output voltage and to the reduced blocking voltage requirement for the switching devices. Presently, these inverters consist of series configurations of fundamental building blocks, each supplied by dedicated, constant DC voltage sources. The inverters have been examined in both symmetric and asymmetric operation modes to generate an expanded palette of voltage levels. The present study extends this architecture by replacing the conventional DC voltage sources with photovoltaic (PV) cells, whose output voltages vary with solar irradiation. The work of Takahashi and Yoshiharu (2002) provides the guiding framework for employing Maximum Power Point Tracking (MPPT) to extract optimal voltage from the PV source. Given that the input to the multilevel inverter should ideally remain constant, a flyback forward converter is interposed between the PV array and the inverter to stabilize the input voltage while accommodating the non-constant solar output. The flyback converter delivers a set of multiple constant output voltages, which the multilevel inverter then expands to a total of 49 discrete voltage levels. The combined system is analyzed to quantify both the total power dissipation within the switching devices and the Peak Inverse Voltage (PIV) experienced. The theoretical predictions are validated through a comprehensive simulation conducted in MATLAB. Results have been confirmed via experiments using bench-scale prototype systems.*

Keywords - *Converter loss, Photovoltaic cell, Multilevel Inverter, DC link voltage, Peak Inverse Voltage.*

1. Introduction

The operational impacts of photovoltaic (PV) generation systems are gaining attention due to their rapid adoption in recent years. Like any electronic system, photovoltaic (PV) systems are defined by their input voltages and currents. There is a wealth of research done to improve efficiency, features, and metrics of PV systems of multiple inputs with higher Maximum Power Point (MPP) capabilities for tracking [1].

The MPPT algorithm's constant DC output voltage forms the forward converter input, which further divides the given constant DC voltage into multiple output voltages necessary operation in asymmetric mode to increase the levels produced on the inverter side [2]. The main interest with respect to the forward converter is the RCD snubber circuitry that is used for the reduction of ripples on the output side of the converter [3]. This allows the multilevel inverter that is supplied with the output of the converter to work with a ripple-free input [4].

Multilevel Inverters (MLIs) are one of the most interesting and promising power conversion solutions employed in renewable energy systems, which are known for their high-quality output voltage, less harmonic distortion, lower electromagnetic interference and high efficiencies [5]. Recently, the objective of the research has been to decrease the number of semiconductor switches and increase the number of output voltage levels of PV applications [6].

The conventional topologies, such as diode clamped and flying capacitor, yield acceptable voltage quality, but involve too many passive components and experience the problems of capacitor voltage balancing [7]. Because of its modular structure, fault tolerance and isolated PV source applicability, Cascaded H-Bridge (CHB) multilevel inverters have been considered [8]. The first type of MLI single-phase transform multilevel inverter is the Diode-Clamped. It has the clamping diodes, which control the voltage levels. In its design, which

is known as the “neutral point” connection, the anodes of the upper diodes are connected to the midpoints of the upper capacitor pairs, and their cathodes are connected to the midpoints of the upper diodes [9]. A variation called the “Capacitor-Clamped MLI” replaces diodes with capacitors. This adds extra bulk to the inverter, leading to cost increases as the capacitors need to be much larger in value to fulfill the need for voltage balance [10]. Bridging these two is the Cascaded H-Bridge MLI, which does not suffer from these issues as it supplies a separate DC source for each H-bridge module [11]. It is very much in demand in the mid-voltage high power markets as it can generate three voltage levels, zero, negative, and positive [12]. It consists of a single-phase full-bridge inverter with its multilevel output connected to its DC source [13]. It is capable of forming single-phase multilevel outputs [14].

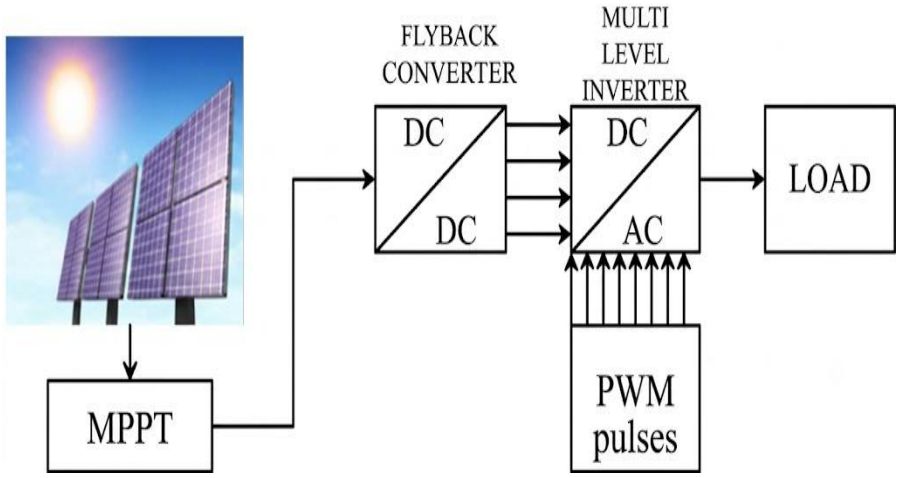


Fig. 1 Proposed 49-level output voltage system

Numerical computations for the IGBT switch quantity, the isolated DC supply, power dissipation, and the output voltage total harmonic distortion have exhibited strong concordance with the results of two additional verification techniques [15]. Contemporary multilevel topologies are being targeted for operation at low switching frequencies and with high-power semiconductor devices, applications extending from Flexible AC Transmission Systems (FACTS) to traction in electric vehicles. The pivotal advantage of multilevel inverters lies in their capacity to efficiently interface with distributed renewable sources, particularly photovoltaic arrays, thereby augmenting overall system performance [16].

This paper introduces a universally applicable multilevel inverter architecture formed by cascading identical modular units, collectively termed the multilevel inverter. Such a configuration raises the attainable output voltage levels sufficiently to lower the voltage stress on individual switching devices while still producing a nearly sinusoidal output, as illustrated in Figure 1. Simulation results prepared in MATLAB, complemented by hardware verification from a laboratory prototype, substantiate the theoretical predictions.

Although the asymmetric Multilevel Inverter (MVI) topologies have progressed to great levels, there are still some practical issues that need to be resolved. The majority of the reported converters either upscale the number of semiconductor switches as the voltage levels go up or need several isolated DC sources with high total standing voltage and Peak Inverse Voltage (PIV). Furthermore, there are a large number of PV-fed multilevel inverter topologies which do not offer adequate control of the varying PV voltage that results from PV solar irradiance fluctuations when switching the PV voltage to inverter stages. Over the years, there have been very few publications about the use of a flyback converter along with an asymmetric cascaded H-bridge multilevel inverter. Hence, a PV-fed MLI with a minimum number of voltage levels, minimum number of switches, minimum TSV, minimum PIV, low harmonics distortion and a high PV conversion efficiency is still required.

The cascaded asymmetric multilevel inverter has significantly reduced the THD; however, it still requires more semiconductor switches, isolated DC sources and higher Total Standing Voltage (TSV). Most of the current topologies are also complex, have high switching losses and low efficiency for changing solar irradiation. While a flyback converter is a galvanically isolated converter with multiple regulated outputs, little research has combined a flyback converter with an asymmetric CHB multilevel inverter for photovoltaic applications. Thus, for reducing the number of switches, TSV, PIV and harmonic distortion, a compact topology with 49 levels to achieve a high efficiency solution is still an open research problem. The problem of reducing switch count, total standing voltage, PIV and regulating PV-fed multilevel operation using a flyback converter has been studied separately in the existing literature.

2. 49 Level Multilevel Inverter

Applications of solar energy have expanded markedly in recent decades, a trend facilitated by the falling cost trajectories of photovoltaic modules and by steady gains in the conversion efficiencies of solar collectors. Additional advantages, including both prolonged operational lifetimes and sustained high energy yields, further justify the technology's adoption. The present study examines a photovoltaic power stage that incorporates advanced Maximum Power Point Tracking (MPPT) techniques, focusing on the perturb and observe (P&O) algorithm, which optimizes the output current supplied to a flyback multi-output converter [17]. The converter is supplied by a multifunctional photovoltaic cell architected to deliver the discrete voltage and current profiles required by a multilevel inverter [18]. An RCD (resistor-capacitor-diode) snubber is deployed on the flyback device to attenuate high-voltage spikes that can otherwise damage the primary-side switching element [19]. The multi-output converter feeds four distinct DC voltage sources within the inverter circuitry, thereby enabling the formation of 49 discrete voltage levels. This structuring contributes to reduced Total Harmonic Distortion (THD) and facilitates the quantification of both conduction and switching losses, as well as the Peak Inverse Voltage (PIV) experienced by the semiconductor components [20].

To address the above drawbacks, in this paper, a PV-fed asymmetrical cascaded H-bridge multilevel inverter along with a multi-output flyback converter is proposed. In the existing PV-fed CHB converter, the voltage regulation and multiple isolated DC voltage generation are done by a single flyback converter. Compared to existing asymmetric topologies, the proposed topology allows for the generation of 49 output voltage levels with just 12 IGBT switches and 4 isolated DC sources, thus reducing the number of components, switching losses, total standing voltage and peak inverse voltage.

Moreover, the proposed inverter demonstrates 360 V output voltage having only 1.87% THD, 98.3% overall efficiency, 0.19 W conduction loss and 0.45 W total power loss. The proposed topology is found to be very well applicable to compact-size power conversion applications for PV systems with excellent power quality and high efficiency.

2.1. Photovoltaic cell

Solar energy is widely accepted as a significant renewable energy resource due to its virtually limitless availability and a cost profile that is effectively zero at the point of capture [21]. Due to not requiring fuel, polluting, and requiring less maintenance, photovoltaic generation is becoming more and more important [22]. Photovoltaic generation exhibits inherent intermittency, with peak output contingent upon both ambient temperature conditions and incident solar irradiance [23].

The PV array consists of a p-n semiconductor junction, and its V-I characteristic can be modeled as (1),

$$I = I_{sc} - I_0 \left\{ exp\left| \left(\frac{q(V+R_S I)}{nKT_k} \right) - 1 \right\} \frac{V+R_S I}{R_{sh}} \quad (1)$$

Where:

I_o = Reverse saturation current,
n = Ideality factor, dimensionless,
R_h, R_s = shunt and Series resistance of the cell,
I_{sh} = Short-circuit current,
T_k = Absolute temperature, Kelvin,
k = Boltzmann constant,
q = Elementary charge.
V,I = Output voltage and output current of the photovoltaic cell.

The circuit configuration of the photovoltaic cell is illustrated in Figure 2.

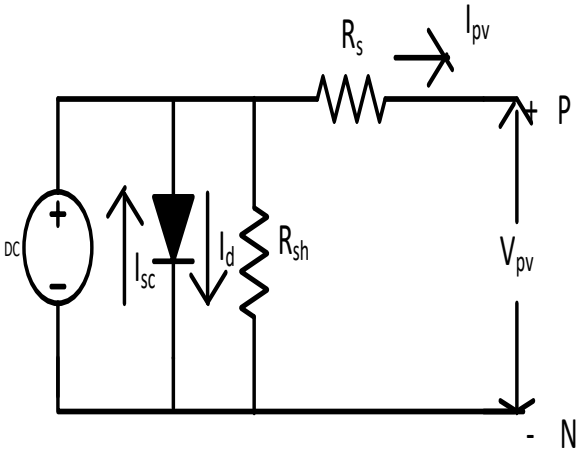
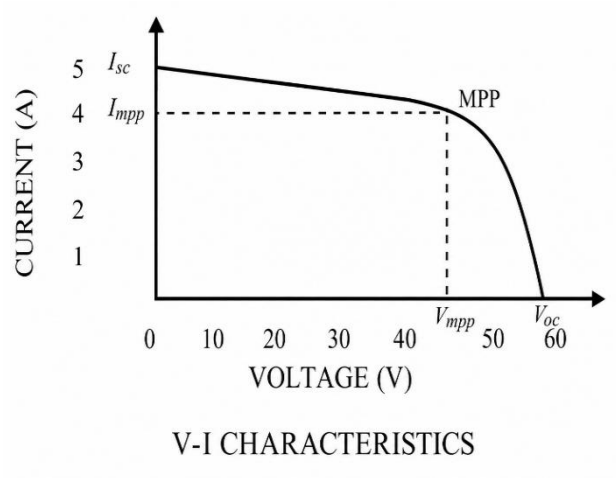


Fig. 2 Schematic diagram of a solar cell

The V-I characteristics and P-V characteristics of the solar cell can be drawn as



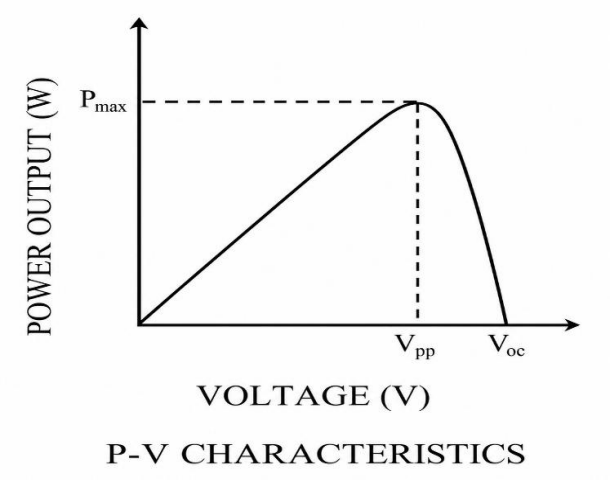


Fig. 3 PV cell diagram and graphs

Maximum Power Point Tracking (MPPT) systems are currently the most effective for ensuring maximum particulary from solar systems as illustrated in Figure 3. External factors like temperature and irradiance are constantly changing and will keep shifting the V-I curve up or down. Increasing temperature will decrease output voltage, and increasing irradiance will affect output current [24].

Fuzzy logic, neural networks, and pilot cells are all examples of MPPT methods. However, if the implementation cost is restricted, then the most suitable methods are Incremental Conductance and P&O.

2.2. Perturb and observe

Figure 4 is an example of an MPPT algorithm based on feedback control and measured parameters of the P & O algorithm. Each modular voltage of the PV cell creates a perturbation that yields an output response. This output power is a response of the solar module output and may vary considerably. The power is adjusted in accordance with the perturbation and will temporarily hold some amount of its constant output [25]. Once the peak power is reached, the condition MPP's power goes to zero output, which throttles the workings of perturbation. The algorithm is said to be oscillating around the peak power in the condition of stability. Hence, in such cases where the feedback perturbation is restricted to minute values, the variation of power should be constrained.

An advanced MPPT method like Incremental Conductance, Fuzzy Logic Control, Artificial Intelligence-based methods like Artificial Neural Networks (ANN) and Particle Swarm Optimization (PSO) can track higher when sun intensity is fluctuating rapidly, but it has higher computational complexity and costs. The Perturb and Observe (P&O) algorithm, however, has a simple control structure, low computation complexity and good tracking performance when uniformly irradiated. The small steady-state oscillations due to the P&O algorithm do not have a significant effect on the system, as the DC-link voltage supplied to the multilevel inverter is controlled. So, the P&O algorithm was chosen because of its practical and economical solution for the proposed photovoltaic-fed multilevel inverter.

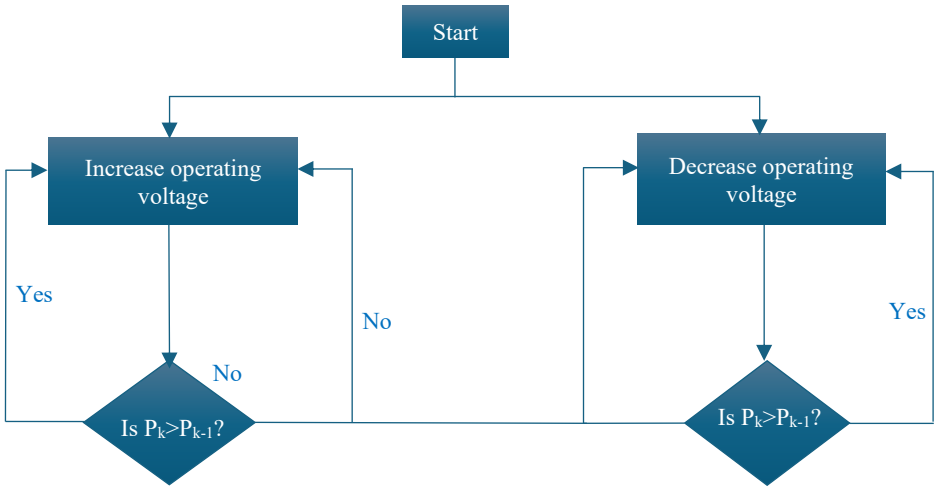


Fig. 4 P&O flowchart

where

P_K = Power Value (Current)

P_{K-1} = Acquired Power Value (Previous)

2.3. Flyback Converters

The voltage source feeds the forward flyback converter. In flyback operation, energizing the switch transfers energy from the magnetizing inductance of the primary and secondary positioned at the output. Discontinuing the switch interrupts the energy transfer, causing the primary energy to generate high leakage voltage spikes that threaten switch integrity. RC snubbers, arranged in parallel with the power switches, mitigate these spikes by dissipating the excessive energy. The flyback topology closely resembles a buck-boost

configuration employing an IGBT in series with a recovery diode. Conceptually, an ideal transformer connected in parallel to the magnetizing inductance aids in visualizing the operation: the transformer magnetizing inductance serves both energy storage and coupling. Under steady-state operation, magnetic circuit analysis enforces volt-second equilibrium, ensuring that the time-averaged voltage across each transformer winding sums to zero.

The circuit illustrated in Figure 5 represents the fundamental arrangement of a flyback converter. The switching period in continuous conduction mode with transistor Q1 permits accumulation of magnetic energy within the magnetizing inductance Lm. Upon forward conduction of diode D1, the previously stored energy in Lm is discharged, causing a redistribution of magnetic flux that delivers energy to the load. The instantaneous output current and voltage levels upon discharge are determined by the output load impedance and the 1:n voltage turns ratio of the transformer.

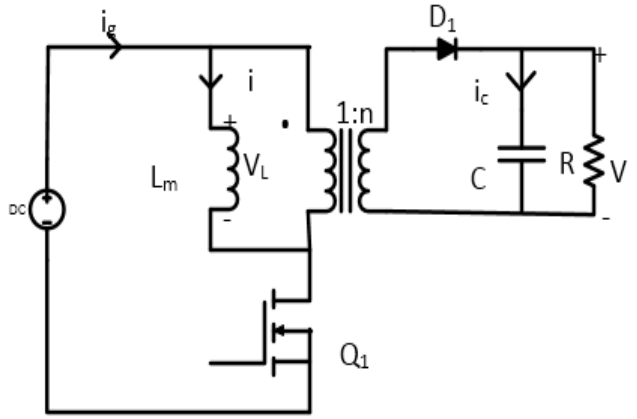


Fig. 5 Single-output flyback converter

Where

L_m is the Magnetizing inductance, D_1 is the Diode, and Q_1 is the IGBT.

This way, we can determine inductor voltage VL, dc source current ig, and capacitor current i_c using Equations (2)-(4) as follows:

$$V_L = V_g \tag{2}$$

$$i_c = -\frac{V}{R} \tag{3}$$

$$i_g = I \tag{4}$$

Let us confirm that if the Q1 switch is opened, and the diode remains conductive, the inductor voltage V_L, the capacitor discharge current, i_c, and the current from the dc source i_g can be determined from the Equations (5)-(7) as follows:

$$v_L = -\frac{V}{n} \tag{5}$$

$$i_c = \frac{I}{n} - \frac{V}{R} \tag{6}$$

$$i_g = 0 \tag{7}$$

The flyback topology proves advantageous in the 50–100 W power spectrum and in the elevated-voltage supplies mandated by CRT-based televisions and computer displays. Its capacity to furnish multiple isolated outputs with a minimal inventory of discrete components is particularly compelling; each additional output is realized through the incorporation of a secondary winding, a rectifying diode, and a filter capacitor. During peak operational transients, the voltage appearing across the power switch is a summative result of the nominal input dc voltage, the output voltage, and the resonant overshoot attributable to the transformer's leakage inductance. Occasionally, a damped snubber network is required to restrain the peak voltage excursion, ensuring it remains below the switch's absolute maximum rating. The specific converter topology employed in this investigation is illustrated in Figure 6.

The Averaged Switch-based Flyback converter modelling using the technique can generally follow two paths. The first path takes the output load and transforms it back to the primary side, thereafter substituting the FET and diode with linearized, perturbed representations of the PWM switch. While theoretically sound, this method is frequently criticized; the derivation of the corresponding Averaged Model consumes far more effort than is saved, given that the linearized FET and diode representations can be obtained with far lower investment of time and complexity. The second path avoids this loading step and seeks to derive the Averaged Model directly.

Although this approach is conceptually more direct, it tends to yield a structure that is algebraically more elaborate than that obtained via the PWM switch path; the additional complexity often offsets the anticipated simplicity of skipping the loading step. Given these comparative labor and complexity costs, the PWM switch approach is favored when the modeling task involves Flyback converters that contain secondary stage LC output filters.

Accordingly, the output impedances Z_1 through Z_4 can be systematically calculated by execution of Equations (8) through (11), wherein the explicit dependence on duty cycles, magnetizing inductance, and filter capacitances is carefully maintained.

$$Z_1 = {}^{V_{01}}/_{I_{D1}} \tag{8}$$

$$Z_2 = {}^{V_{02}}/_{I_{D2}} \quad (9)$$

$$Z_3 = {}^{V_{03}}/_{I_{D3}} \quad (10)$$

$$Z_4 = {}^{V_{04}}/_{I_{D4}} \quad (11)$$

Thus, the output from the converter is being given as the input to the multilevel inverter.

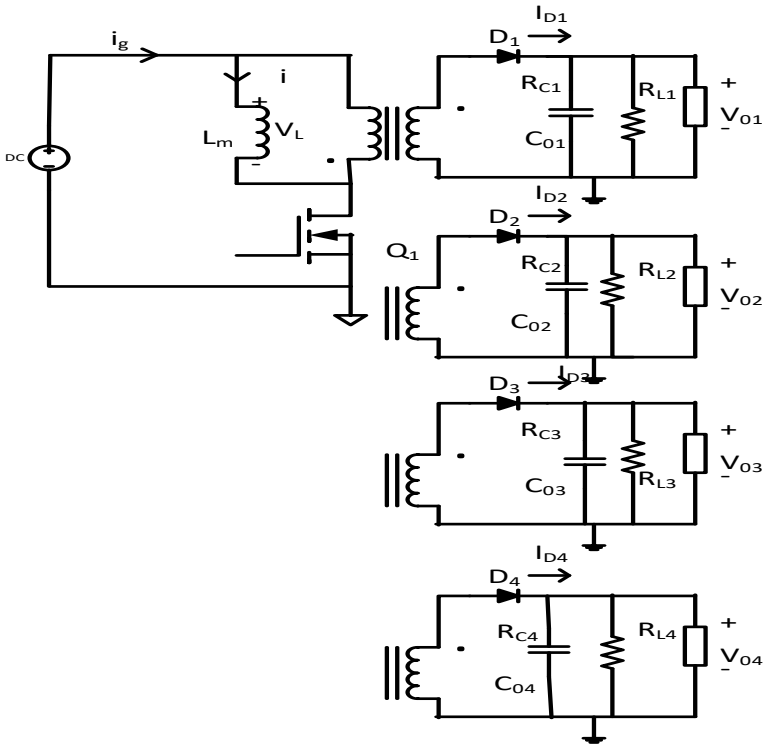


Fig. 6 Multi-output of flyback converter circuit

3. Fundamental Block of the Proposed Inverter

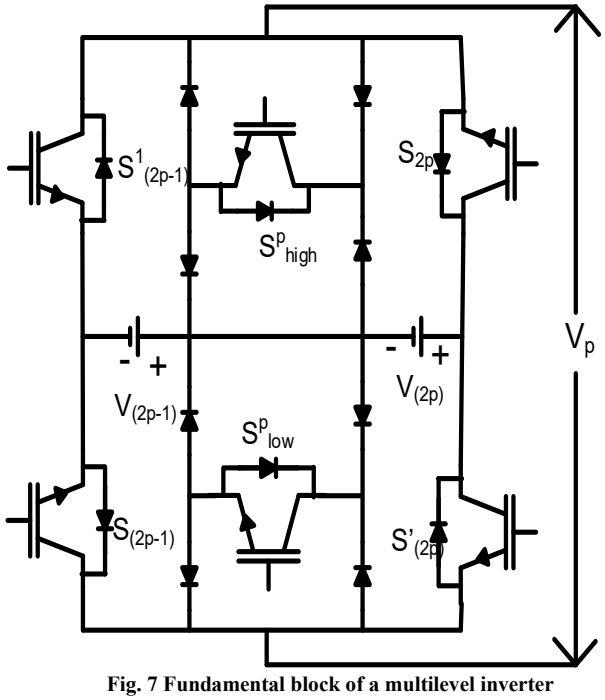


Fig. 7 Fundamental block of a multilevel inverter

The basic block of the proposed multilevel inverter equipped with two DC voltage sources is shown in Figure 7. When both sides of a voltage source are given the same value, then we say that the device is working in symmetric mode. On the other hand, if the supplied voltage is found to be different, then the device is operating in an asymmetric mode of operation.

This block contains 6 semiconductor switches associated with the diodes installed in antiparallel configuration. It also contains 8 of the diodes, which are responsible for the conduction of the backward current, which is induced due to the inductive nature of a load. The semiconductor switches used in this circuit is IGBT. Above circuits contain different blocks, which are required for different levels of operation. If we consider the blocks to be first, 'p' value is set to 1, then the switches will be S_1, S_2, S_2^1, S_1^1, S_{low}^1, S_{high}^1, V_2, and V_1.

3.1. Symmetric Mode

All DC sources are set to V in the symmetric mode of operation. Five levels of output voltage are achievable. With the correct sequence of turning the switches on and off, positive and negative voltages, as well as zero voltage, can be achieved in Table 1.

Table 1. Symmetric mode switching states

State	Output Level	Switches ON (Possible Combinations)	Output
1	+2	S1 and S_2	+2 V
2	+1	(S_1 and S_{high}^1) or (S_2 and S_{low}^1)	+1 V
3	0	(S_{low}^1 and S_{high}^1) or (S_2 and S_2^1) or (S_1 and S_1^1)	0 V
4	-1	(S_1^1 and S_{low}^1) or (S_2^1 and S_{high}^1)	-1 V
5	-2	S_1^1 and S_2^1	-2 V

Regarding the correct device switching, approximate average power control by the switching state redundancy is determined with Equation (12).

$$V2p = V(2p-1) = V \quad (12)$$

3.2. Asymmetric mode

The output voltages-three positive, three negative, and one neutral-can be classified into seven distinct levels in the asymmetric mode in Table 2. Furthermore, the input voltages applied to the sources need not be the same and are asymmetric in nature. The configuration is given in [8]. The output levels can be calculated using (13).

$$V2p = 2V(2p-1) \quad (13)$$

Table 2. Asymmetric mode switching states

Row	Output Voltage	S_1 (ON)	S_2 (ON)	S_{low} (ON)	S_{high} (ON)
1	+3V	on	on	off	off
2	+2V	off	on	on	off
3	+1V	on	off	off	on
4	0V	off	off	on	on
5	-1V	on	off	on	off
6	-2V	off	on	off	off
7	-3V	on	on	on	off

3.3. Proposed multilevel inverter

A generalized multilevel inverter is an electrical circuit that generates a stepped or staircase-like AC output voltage waveform by combining several simpler inverter units, known as fundamental inverter blocks. The core idea behind this design is to achieve a smoother, more sinusoidal output voltage using voltage sources of multiple DC and switching elements.

Here, two fundamental topologies are arranged in series, and the configuration is purposely driven in the asymmetric modulation mode, enabling the output voltage to theoretically attain 49 distinct levels.

To realize the required raster of voltages, a suite of DC voltage supplies is deployed, with the appropriate magnitudes being derived through the formulation expressed in (14).

$$V(r) = \begin{cases} 7^{\left[(r-1)/2\right]}V; & for\ r: odd \\ 2X7^{\left[(r-2)/2\right]}V; & for\ r: even \end{cases} \quad (14)$$

r= Number of DC Voltage sources

Here, for two blocks, the values are found to be $V_{(2)}$=2V; $V_{(1)}$=V; $V_{(4)}$=14V; $V_{(3)}$= 7V.

The block diagram of the proposed system is shown in Figure 8.

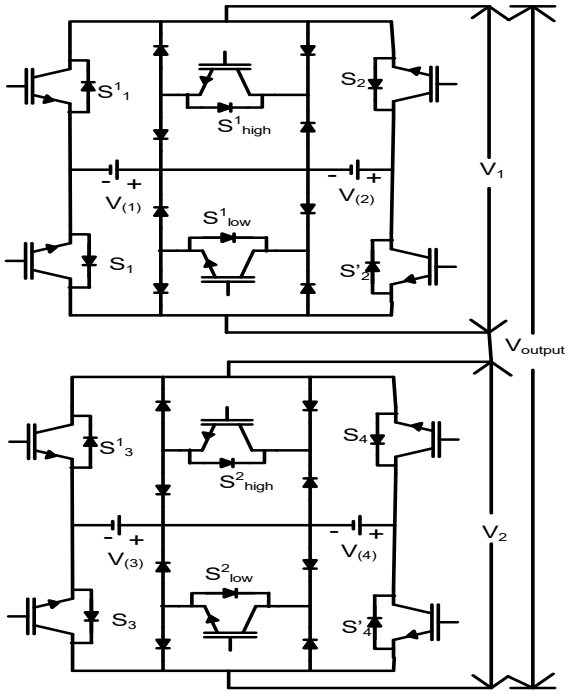


Fig. 8 49-level inverter developed topology

Block output voltages may be determined according to the values provided in Table 3. The block produces a total of 49 voltage levels characterized by 24 positive levels, 24 negative levels, and a zero voltage level.

In the initial level, S_1, S_2, S_3, and S_4 switches are closed, whereas eight other switches remain open. Switches S1 and S2 contribute a voltage of 3 V, while S_3 and S_4 contribute 21 V; therefore, the cumulative voltage output at the first level is 24 V.

Table 3. Output voltage of two blocks

Level State	Level	ON State Switches	Voltage output
1	+24	S_1,S_3,S_4,S_2	+24V
2	+23	S_3,S_{low}^1,S_4,S_2	+23V
3	+22	S_3,S_{high}^1,S_4,S_1	+22V
4	+21	$S_{high}^1, S_3,S_4,S_{low}^1$	+21V
5	+20	S_1^1,S_{low}^1, S_3,S_4	+20V
6	+19	$S_2^1,S_{high}^1, S_3,S_4$	+19V
7	+18	S_1^1,S_2^1, S_3,S_4	+18V
8	+17	S_1,S_2,S_4,S_{low}^2	+17V
9	+16	$S_2,S_{low}^1, S_4,S_{low}^2$	+16V
10	+15	$S_1,S_{high}^1, S_4,S_{low}^2$	+15V
11	+14	$S_{high}^1,S_{low}^1, S_4,S_{low}^2$	+14V
12	+13	$S_1^1,S_{low}^1, S_4,S_{low}^2$	+13V
13	+12	$S_2^1,S_{high}^1, S_4,S_{low}^2$	+12V
14	+11	$S_1^1,S_2^1, S_4,S_{low}^2$	+11V
15	+10	S_1,S_2, S_3,S_{high}^2	+10V
16	+9	$S_2,S_{low}^1, S_3,S_{high}^2$	+9V
17	+8	$S_1,S_{high}^1, S_3,S_{high}^2$	+8V
18	+7	$S_{high}^1,S_{low}^1, S_3,S_{high}^2$	+7V
19	+6	$S_1^1,S_{low}^1, S_3,S_{high}^2$	+6V
20	+5	$S_2^1,S_{high}^1, S_3,S_{high}^2$	+5V
21	+4	$S_1^1,S_2^1, S_3,S_{high}^2$	+4V
22	+3	$S_1,S_{low}^2,S_{high}^2,S_2$	+3V
23	+2	$S_2, S_{low}^2,S_{high}^2,S_{low}^1$	+2V
24	+1	$S_1, S_{low}^2,S_{high}^2,S_{high}^1$	+1V
25	0	$S_{high}^1, S_{low}^2,S_{high}^2,S_{low}^1$	0V
…	…	…	…
49	-24	S_3^1,S41,S11,S_2^1	-24V

The expression for determining the number of levels is derived from Equation (15) as follows:

$$N_{level} = 7^p \quad (15)$$

where p denotes the number of blocks. Give $n_p = 2$ for this example, the system is configured to yield 49 distinct voltage levels. The corresponding maximum and minimum voltage values can, accordingly, be determined via the equation designated as in Equation (16).

$$V_{max} = +\frac{1}{2}(7^p - 1)V \quad (16)$$

Substituting the value of p= 2 reveals that the maximum voltage delivered by the block is measured to be +24V in Equation (17).

$$V_{min} = -\frac{1}{2}(7^p - 1)V \quad (17)$$

The analysis established a minimum voltage threshold of -24 V for the system under the parameters described above.

The required number of Insulated-Gate Bipolar Transistors (IGBTs) and associated power supply units within the design can be determined by implementing Equations (18) and (19).

$$N_{IGBT} = 6p \quad (18)$$

$$N_{source} = 2p \quad (19)$$

From the preceding calculations, the number of required components for the system has been quantified as twelve IGBT switches and four DC voltage sources.During the operation of the IGBT switches, the second stack voltage has been found to remain steady whenever the output voltage of the first stack stabilizes, exhibiting this steady-state behavior periodically every seven switching states. As a consequence, a control frequency of comparatively low value suffices to govern the states of the switches in the second stack, thereby leading to a reduction in implementation costs. Given the application of a single-phase DC voltage source, the maximum allowable voltage has been constrained to 230 V, resulting in a permissible peak voltage limit of 10 V for this circuit.

Figure 9 presents the finalized circuit architecture of the proposed system, encompassing the photovoltaic module, the flyback converter stage, and the multilevel inverter stage.

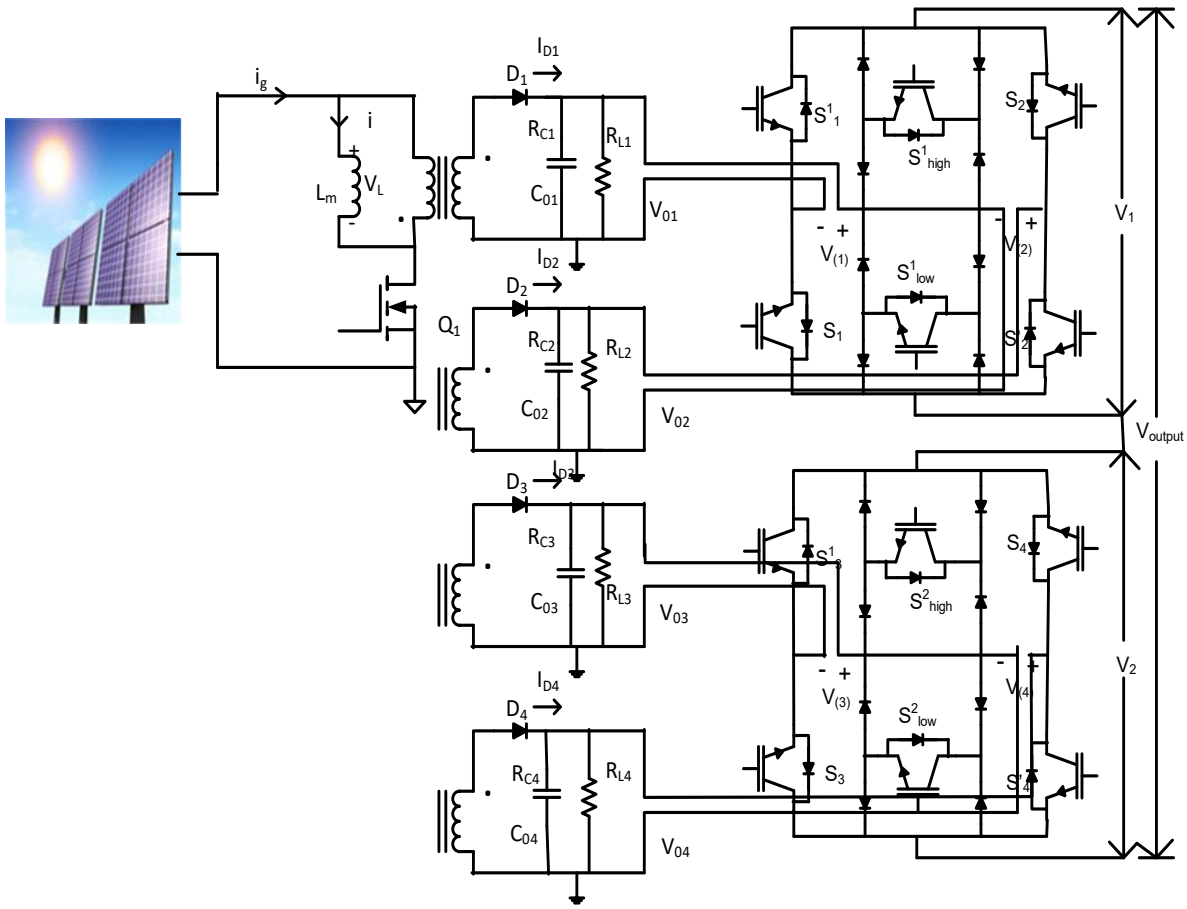


Fig. 9 Proposed cascaded H-bridge inverter with 49 levels

4. Losses Calculation

Total power loss in a power electronic switch, such as an IGBT or diode, is a critical parameter for system design and efficiency analysis. This loss is a combination of three main categories: conduction losses, blocking losses, and switching losses. Conduction losses, also known as on-state losses, are dissipated when the switch is in the fully ON state and is conducting current. These losses arise primarily from the equivalent on-state resistance of the device. Even though an ideal switch has zero resistance when on, real-world components have a small, non-zero resistance. According to Joule's law, power dissipated is the product of the square of the resistance and current. Therefore, conduction losses are directly proportional to the current switch. This makes them a significant contributor to total losses, especially in high-current applications. Switching losses occur during the transition between the OFF and ON states (and vice versa). This is a dynamic process where both the current through the switch and the voltage across the switch are non-zero simultaneously.

A typical switching cycle involves a turn-on and a turn-off phase. During turn-on, the current increases while the voltage across the switch decreases. During turn-off, the voltage increases while the current decreases. The instantaneous power loss is the product of the instantaneous current and voltage. The total energy lost during one switching cycle is the integral of this power over the switching time. Since this loss occurs with every switching event, the total switching power loss is dependent on the switching frequency. Higher switching frequencies lead to more frequent transitions and, consequently, higher switching losses.

Blocking losses, or off-state losses, are the power losses that occur when the switch is in the fully OFF state and is blocking voltage. In this state, an ideal switch would have infinite resistance and zero current flow. However, real switches have a small, non-zero leakage current that flows through the device even when it is turned off. The power loss is the product of the voltage across the device and this leakage current. In most applications, this leakage current is extremely small (on the order of microamperes), which makes the resulting blocking losses negligible compared to conduction and switching losses. Consequently, blocking losses are often omitted from total power loss calculations for practical purposes, as in (20).

$$P_{loss} = P_{cond} + P_{Switch} \tag{20}$$

4.1. Conduction loss

During the period in which the IGBT transitions to the on-state and current traverses the device, conduction losses are registered as the total power dissipated in the on-state, quantified as the product of the on-state resistance and the on-state current. Under PWM control, these losses are instead scaled by the mean output current seen over the half-cycle. The average power dissipation in the IGBT may thus be expressed as in (21)

$$V_{ds}(i_D) = R_{Dson}(i_D).\, i_D \tag{21}$$

Where,

R_{Dson}=On-state resistance of MOSFET

i_D→ On state current

From this, the conduction loss through the switch can be calculated by multiplying the voltage obtained by the on-state current, as shown in (22)

$$P_{CM(T)} = V_{ds}(i_D) * \ i_D \tag{22}$$

Where,

$V_{ds}(i_D)$ → on state voltage

The conduction loss through the diode can be defined as the product of on state voltage across the diode and on state current through the diode, as shown in (23)

$$P_{Cond.d} = V_D(t) * \ i_D(t) \tag{23}$$

For substituting in this above equation, the value of on state voltage across the diode can be calculated as (24)

$$V_D(t) = \ V_{D0} + R_D * i_D \tag{24}$$

Where,

R_D→Diode resistance

i_D→ On-state diode current

Using the above Equations (21)-(24), the total conduction loss of the circuit can be found as (25)

$$P_{cond.total} = P_{CM(T)} + P_{cond.d} \tag{25}$$

By using the datasheet values for the parameters used in the above equation, the total conduction loss power in the proposed circuit has been found to be 0.19W, which is found to be lower than the existing system that is present.

4.2. Switching loss

Switching losses are the losses that normally occur during the turn-off and turn-on period of the switch [16]. Therefore, energy loss during the turn-on and off period of the switch (26) through (29) can be calculated as,

$$\mathrm{E_{on,T}} = \int_0^{\mathrm{t_{on}}} \mathrm{v(t)i(t)dt} \tag{26}$$

$$\mathrm{E_{on,T}} = \int_0^{\mathrm{t_{on}}} \left[\left(\frac{\mathrm{V_{switch,T}}}{\mathrm{t_{on}}}.\mathrm{t}\right)\left(\frac{-\mathrm{I'}}{\mathrm{t_{on}}}(\mathrm{t}-\mathrm{t_{on}})\right)\right]\mathrm{dt} \tag{27}$$

$$\mathrm{E_{on,T}} = \frac{1}{6}\mathrm{V_{switch,T}I't_{on}} \tag{28}$$

Similarly,

$$\mathrm{E_{off,T}} = \frac{1}{6}\mathrm{V_{switch,T}I't_{off}} \tag{29}$$

Consequently, the overall switching losses may be quantified employing the expression given by (30).

$$\mathrm{P_{switch}} = 2\mathrm{f}\left[\sum_{\mathrm{k=1}}^{\mathrm{N_{s,w}}}\left(\sum_{\mathrm{i=1}}^{\mathrm{N_{on,k}}}\mathrm{E_{on,k,i}} + \sum_{\mathrm{j=1}}^{\mathrm{N_{off,k}}}\mathrm{E_{off,k,j}}\right)\right] \tag{30}$$

where $f_i$is the fundamental frequency, $E_{\{on,k,i\}}$and $E_{\{off,k,j\}}$ represent the energy loss of switch k during the on and off states, and $\left(N_{\{on,k\}}\right)$and $(N_{\{off,k\}})$ denote the number of turn-on and turn-off transitions of switch k within the half cycle, respectively.

Total power loss in a power electronic switch, such as an IGBT or diode, is a critical parameter for system design and efficiency analysis. This loss is a combination of three main categories: conduction losses, blocking losses, and switching losses.

Conduction losses, also known as on-state losses, are dissipated when the switch is in the fully ON state and is conducting current. These losses arise primarily from the equivalent on-state resistance of the device. Even though an ideal switch has zero resistance when on, real-world components have a small, non-zero resistance. According to Joule's law, power dissipated is the product of the square of the current and the resistance.

Therefore, conduction losses are directly proportional to the square of the current flowing through the switch. This makes them a significant contributor to total losses, especially in high-current applications. Switching losses occur during the transition between the ON and OFF states. This is a dynamic process where both the voltage across the switch and the current through it are non-zero simultaneously. A typical switching cycle involves a turn-on and a turn-off phase. During turn-on, the voltage across the switch decreases while the current increases. During turn-off, the voltage increases while the current decreases. The instantaneous power loss is the product of the instantaneous voltage and current. The total energy lost during one switching cycle is the integral of this power over the switching time. Since this loss occurs with every switching event, the total switching power loss is

dependent on the switching frequency. Higher switching frequencies lead to more frequent transitions and, consequently, higher switching losses.

4.3. Total loss

The aggregate power dissipation may be evaluated employing the expression (31)

$$P_{avg,IGBT} = P_{cond} + P_{switch} \quad (31)$$

From above,
P_{cond}= Conduction loss
P_{swit}= Switching loss

The calculated overall power loss of 0.45Wis considerably less than what was observed in the previous system design.

5. Simulation Output

The electric circuit subsystem of the solar PV panel module includes a DC-DC flyback converter and a P&O algorithm. For the solar PV subsystem, models were developed in MATLAB for power sampling and other functions, which utilized PWM pulses for solar PV MPPT algorithms.The flyback converter and microcontroller receive the current and voltage readings from solar PV modules simultaneously. Furthermore, the duty cycle adjustment is performed via P&O algorithm. For tracking the Operating Point (OP) that is distant from the Maximum Power Point (MPP), high perturbation is applied, and low perturbation is applied for OP near the MPP, as illustrated in Figure 10. The difference in the duty cycle will primarily depend on the actual maximum power tracking-proximity or closeness of a gained tracked power. This depends on how the memory increment value is chosen.

Table 4. MATLAB Simulink simulation parameters

Parameter	Value
PV Module Rated Power	500 W
Open-Circuit Voltage (V_{oc})	50 V
Short-Circuit Current (I_{sc})	13 A
Maximum Power Voltage (V_{mp})	41 V
Maximum Power Current (I_{mp})	12.2 A
Solar Irradiance	1000 W/m²
Cell Temperature	25 °C
Magnetizing Inductance	2 mH
Output Capacitors	470 µF
DC Output Voltages	15V, 30V, 105V, 210V
Output Frequency	50 Hz
Load Type	Resistive Load
Load Resistance	100 Ω
Filter Inductor	3 mH
Filter Capacitor	10 µF
Number of IGBT Switches	12
Number of DC Sources	4
Output Voltage Levels	49

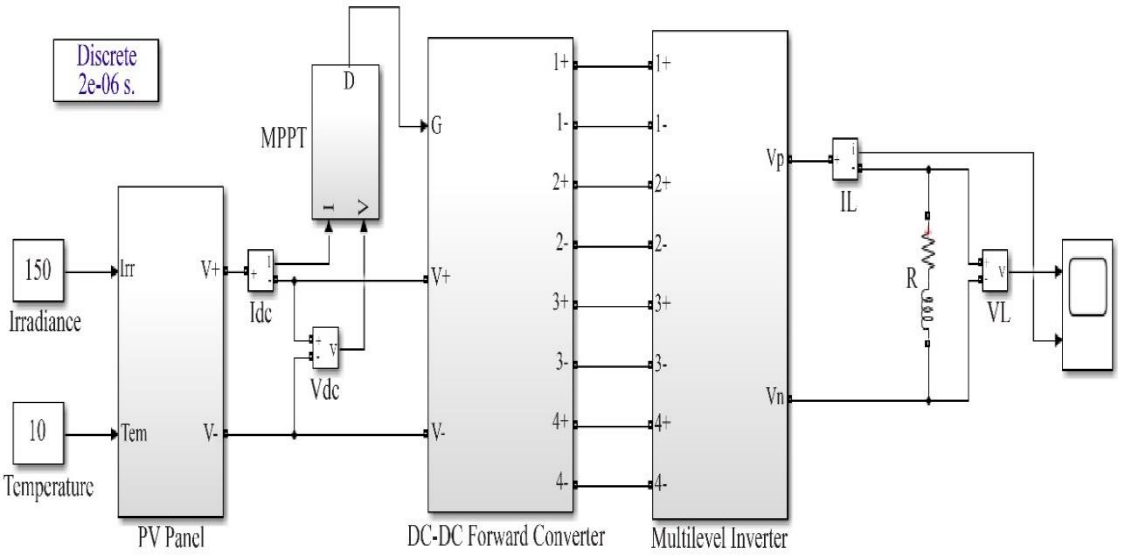


Fig. 10 Flyback converter based MPPT system model in MATLAB

A 49-level asymmetrical cascaded H-bridge multilevel inverter, fed by PV units, was modeled and verified in MATLAB / Simulink. The multi-output flyback converter was controlled by the conventional Perturb and Observe (P&O) MPPT algorithm, and the 500 W PV module was operated at 1000 W/m^2 irradiance and 25°C cell temperature. The asymmetrical CHB inverter was fed by the four regulated 15V, 30V, 105V and 210V DC voltages provided by the flyback converter at a switching frequency of 20 kHz. The inverter used fundamental-frequency switching for the output voltage of 50 Hz and 49 levels. The proposed system was tested with a resistive load of 100 Ω as illustrated in Table 4, and the

results were analyzed in terms of output voltage, output current, THD, blocking voltage, PIV, power losses and overall efficiency.

5.1. Voltage and Current Characteristics

Using MATLAB, I constructed a multilevel inverter model that facilitates in-depth analysis of the output voltage and current waveforms, as well as the corresponding input excitations. This configuration enables a detailed exploration of harmonic content, switching losses, and thermal performance across each component of the inverter stage.

The simulation environment supports parametric sweeps and fault conditions, augmenting the fidelity of design verification.The simulation has consequently yielded an exceptionally close approximation to the desired waveform, thereby enabling the generation of 49 distinct voltage levels. By applying the control strategy labeled D, the required magnitudes of the individual DC voltage sources are derived from Equation (14) and summarized as follows: $V_2 = 30$ V, $V_1 = 15$ V, $V_3 = 105$ V, and $V_4 = 210$ V. The corresponding DC voltage input waveforms, as computed in the MATLAB environment, are presented in Figure 11.

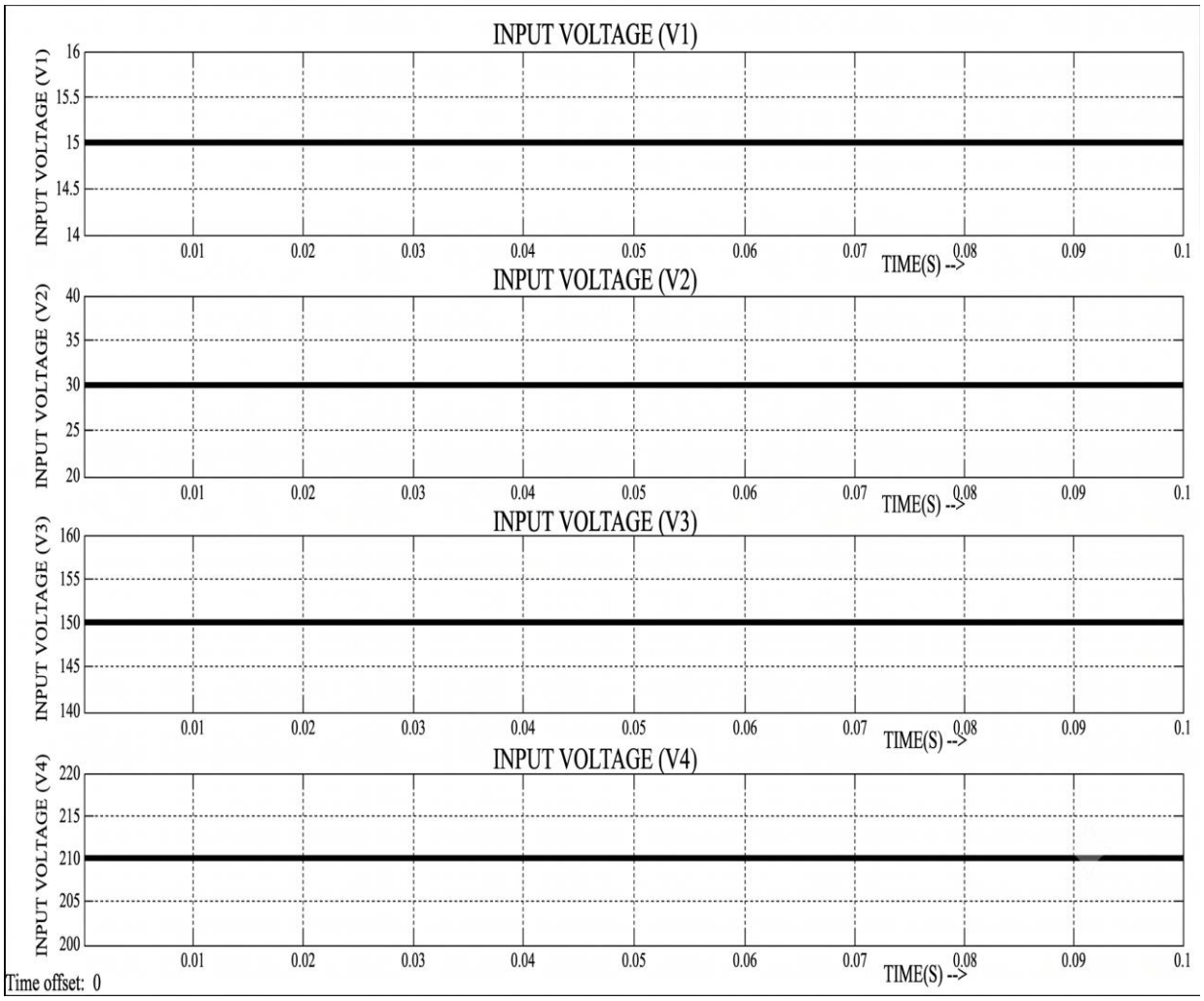


Fig. 11 Voltage waveforms at the inputs of the suggested multilevel inverter topology

Utilizing the supplied input voltages, the proposed configuration output voltage is determined in accordance with Equation (32) as follows:

$$V_0 = V(1) + V(2) + V(3) + V(4) \quad (32)$$

Utilizing the supplied nominal values of the four DC sources, the experimental configuration yielded an output voltage of 360 volts from the 49-level multilevel inverter.

The increased voltage resolution results in significant reduction of harmonic content, as shown in Figure 12, when compared with the conventional topologies with 31 levels of voltage. The measured THD value is 1.87%, which meets IEEE-519 recommendations and indicates better waveform quality.

The proposed 49-level multilevel inverter output current waveform generated is shown in Figure 13.

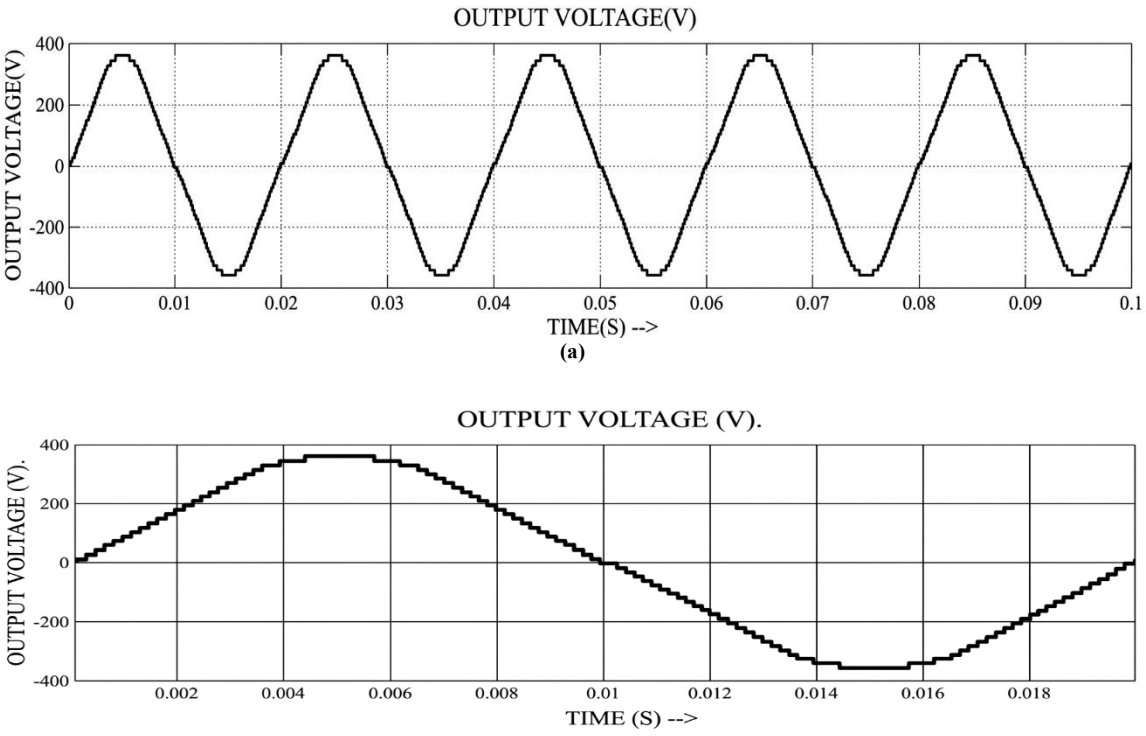


Fig. 12(a) The proposed inverter circuit output voltage, and (b) The proposed 49 Voltage levels output voltage.

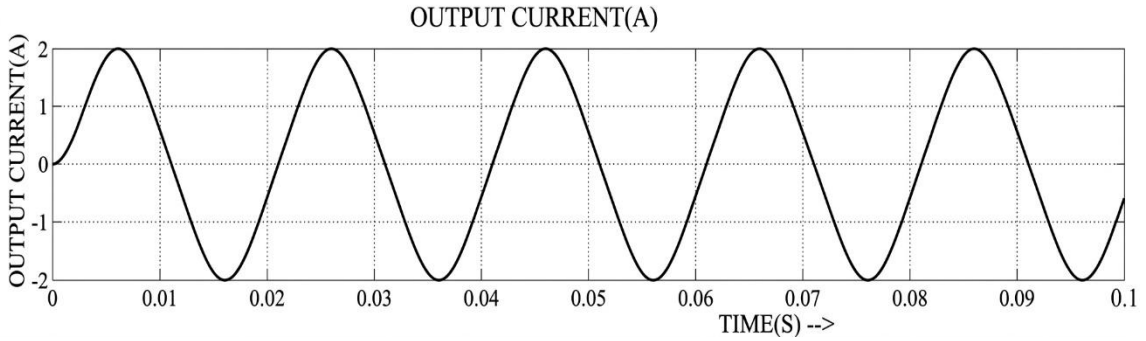


Fig. 13 Proposed multilevel inverter circuit output current

5.2. Total Harmonic Distortion

Total Harmonic Distortion quantitatively characterizes the extent of a waveform's deviation from the ideal fundamental frequency. This metric is quantitatively expressed in Equation (33)

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=2,3}^{\infty} V_n^2} \quad (33)$$

Where,
V_1 = fundamental voltage
V_n = voltage of the nth harmonic component

The overall total harmonic distortion for the proposed 49-level multilevel inverter configuration is calculated to be 1.87%. The corresponding spectral distribution, illustrated in Figure 14, corroborates this result.

The proposed topology consists of a multi-output flyback converter with an asymmetrical Cascaded H-Bridge (CHB) inverter that produces 49 output voltage levels while only requiring 12 IGBT switches and four isolated DC sources, as compared to recent asymmetrical Cascaded H-Bridge (CHB) multilevel inverter topologies, which typically require a larger number of semiconductor switches, complex modulation strategies and multiple independent DC sources for achieving higher output voltage levels. The proposed configuration not only reduces the number of switches, Total Standing Voltage (TSV), Peak Inverse Voltage (PIV), conduction loss and switching loss, but also allows for a THD of 1.87% and the efficiency of 98.3%. The proposed topology is distinguished from recent asymmetrical multi-level inverter designs by a fly-back assisted multiple output DC source and a reduced switch 49-level inverter, which makes it ideally suited to the application in PV systems.

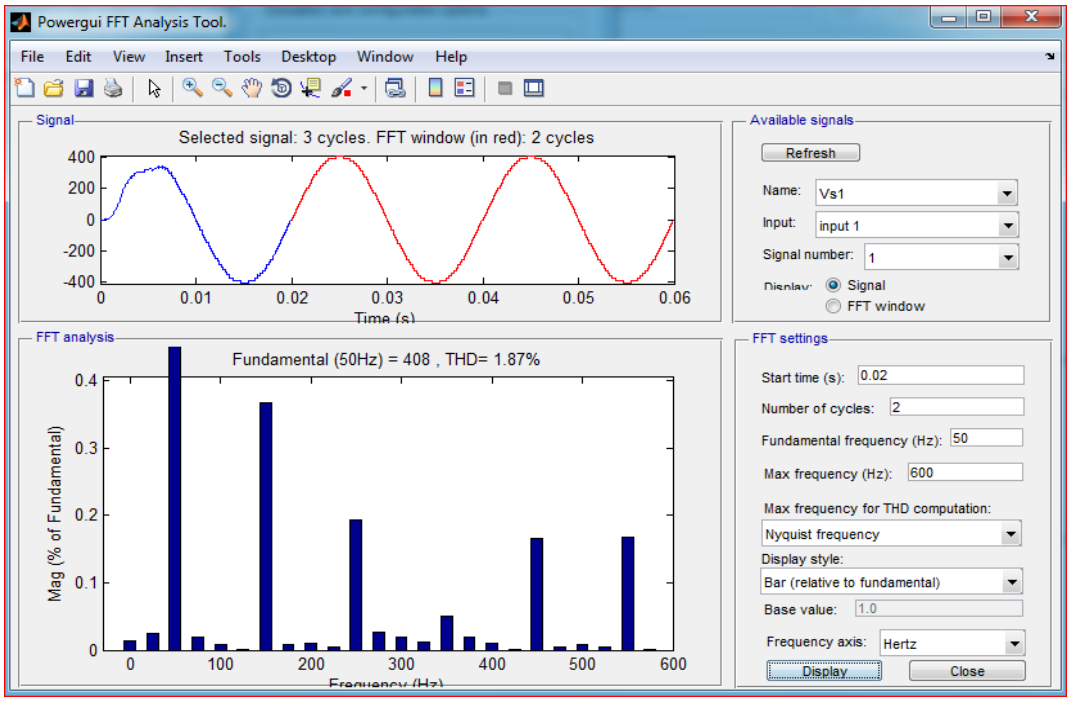


Fig. 14 Multilevel inverter total harmonic distortion

5.3. Blocking Voltage

Reducing the allowable blocking voltage on semiconductor switches is a key factor in lowering the overall cost of inverter design. This is because components with lower voltage ratings are typically less expensive. For the inverter, to find the total blocking voltage, it is necessary to assess blocking voltage on every single switch.For the initial stage of the circuit, the total blocking voltage across switches S1, S1', S2, and S2' is given by a specific relationship. Similarly, the blocking voltage for switches S1 high and S1 low is determined by a separate equation. A specific formula is applied to compute the comprehensive blocking voltage for a 49-level asymmetric arrangement as in (34).

$$V_{bl}^{p} = \begin{cases} 3\,X\,7^{(p-1)}V \;;\; S_{(2p-1)}, S_{(2p)}, S'_{(2p-1)}, S'_{(2p)} \\ 2\,X\,7^{(p-1)}V \;;\; S^{p}_{high}, S^{p}_{low} \end{cases} \quad (34)$$

where V represents the DC voltage supply, and P denotes the number of voltage-dividing blocks (here, P = 2) in the present analysis. Consequently, substituting into Equation (35) enables the determination of the aggregate blocking voltage across the first voltage-dividing block in the proposed configuration, expressed analytically as

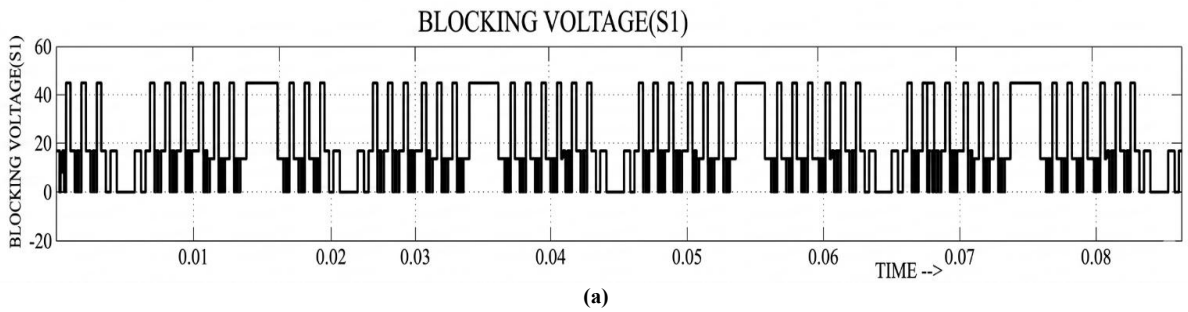
$$Vbltotal = 4(3\,X\,7^{(p-1)}V) + 2(2\,X\,7^{(p-1)}V) \quad (35)$$

In the proposed circuit, two blocks are taken into consideration. So, from this, the total blocking voltage of the proposed circuit (36) can be found and shown in Figure 15.

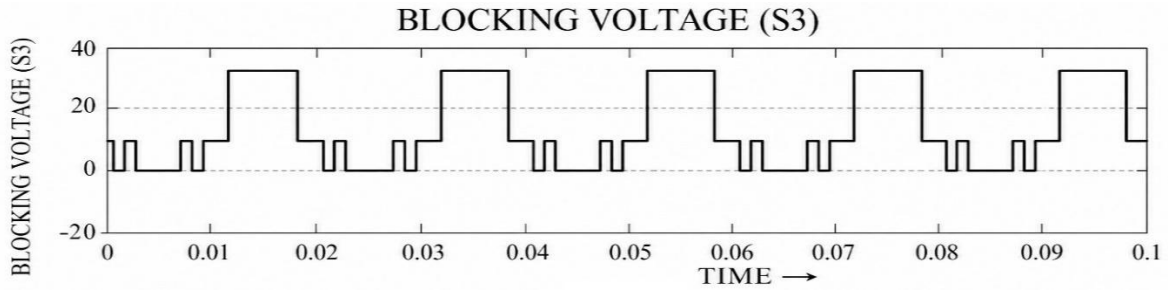
Total blocking voltage

$$Vtotalbl = 2(4(3\,X\,7^{(p-1)}V) + 2(2\,X\,7^{(p-1)}V)) \quad (36)$$

Analysis of the proposed circuit yields a maximum permissible blocking voltage of 10 V for a single switching element.



(a)



(b)

Fig. 15 (a) Switch (S_1)-Blocking voltage, and (b) Blocking voltage of S_3 switch.

5.4. Peak Inverse Voltage

The highest reverse voltage magnitude, named as Peak inverse voltage, is experienced by the diode during its reverse-biased phase, precisely occurring at the apex of the alternating current input waveform. To determine the PIV, the initial calculation required is the standing voltage, commonly designated as the blocking voltage, as in (37).

$$\mathrm{PIV_{total}} = \frac{8}{3}(7^{\mathrm{p}} - 1)\mathrm{V} \tag{37}$$

By manipulation of the preceding expression, the Peak Inverse Voltage (PIV) of the rectifying device may be obtained subsequently:

The normalized Peak Inverse Voltage (PIV norm) may be approximated by the relation as in (38) & (39):

$$\mathrm{PIV_{norm}} = \frac{\mathrm{PIV_{total}}}{\mathrm{V_{max}}} \tag{38}$$

$$\mathrm{PIV_{norm}} = \frac{\frac{8}{3}(7^{\mathrm{p}}-1)\mathrm{V}}{\left(\frac{7^{\mathrm{p}}-1}{2}\right)\mathrm{V}} = \frac{16}{3} \tag{39}$$

5.5. DC Link Voltage

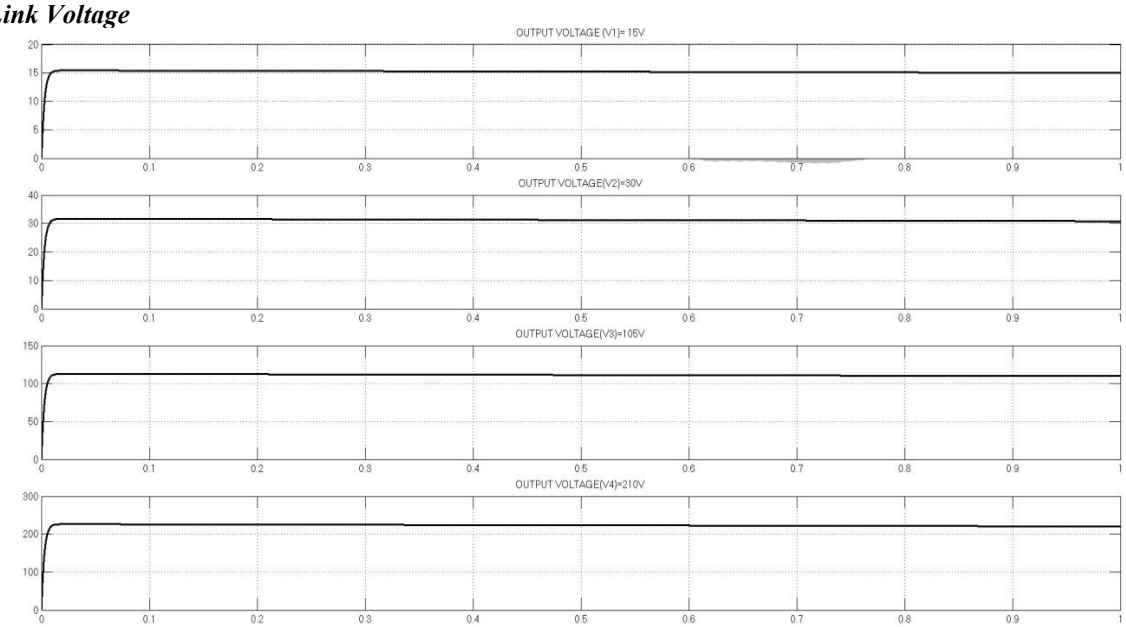


Fig. 16 Converter side DC link voltage

The direct current link voltage is specified as the voltage measured at the junction node between the rectification stage and the inversion stage of a given power electronic drive. For any given drive, the voltage and power levels dictate a specific functional topology; as the rated voltage and power diminish, the overall physical complexity and component count of the drive topology similarly reduce, a trend illustrated in Figure 16. When the drive is characterised by a specified voltage and power rating, the resulting topology incorporates a direct current link stage that includes a storage capacitor, which stabilises the voltage swing occurring between the rectifier and the inverter.

Table 5 provides a comparative assessment of the proposed topology with recently reported PV-fed multi-level inverter topologies, showing benefits in terms of reduced number of switches, voltage levels, harmonic performance and complexity of implementation.

Table 5. Comparison of recent PV fed multilevel inverter topologies

Reference	Topology	Switch Count	Voltage Levels	THD	Limitation
[10]	Reduced-switch MLI	Higher	Lower	Moderate	High TSV
[13]	Switched-capacitor MLI	Higher	17	Low	Capacitor balancing
[14]	CHB Active Filter	High	Medium	Low	High-frequency control
[16]	CHB with SVPWM	High	Medium	Low	Complex modulation
Proposed	Flyback-assisted Asymmetric CHB	12	49	1.87%	Lower switch count, lower TSV

The proposed inverter is tested to ensure stable operation under different input and load conditions: ±1.2% output voltage regulation is demonstrated. The harmonic standard specified in IEEE-519 is met by FFT analysis, which shows a THD of 1.87%. The output voltage and current have low ripple of 0.9% and 1.3%, respectively, because of the high number of voltage levels and regulated DC outputs of the multi-output flyback converter. Moreover, the inverter has a very low power factor of 0.99, which means the supplied power is used very efficiently with very low reactive power demand. The results indicate that the designed topology achieves better voltage quality, less ripple and high power quality, which can be used in the PV power conversion applications.

6. Conclusion

In this paper, we present a 49-level multilevel inverter specifically designed to integrate photovoltaic sources while minimizing semiconductor count and maximizing achievable output voltage levels. A comprehensive examination is provided, addressing total harmonic distortion, maximum blocking voltage, and peak inverse voltage across the inverter stages. Since the architecture incorporates a DC-DC converter, we also derive the DC link voltage imposed across the switching devices. Our analysis confirms the configuration's suitability for high-voltage applications under constraints of minimal switch population. Control of the proposed topology is structured to segregate switch operations into high- and low-frequency domains, thereby attenuating thermal stress, component size, and circuit cost. Dynamic waveforms reveal the inverter synthesizes output levels of 15V, 30V, 105V, 210V, and 310V. Loss models, PIV assessments, and computed figures of merit indicate the design's superior performance relative to existing multilevel configurations. The proposed topology generates 49 output voltage levels with a minimum number of 12 IGBT switches and four isolated DC sources. The inverter can produce the output voltage of 360 V, THD of 1.87%, overall efficiency is about 98.3%, conduction loss (0.19W), total power loss (0.45W) and a small peak inverse voltage compared to the recent asymmetric multilevel inverter topologies. The dynamic simulation confirms stable operation and effective MPPT performance under the load and irradiance variations, proving the suitability of the proposed inverter for photovoltaic grid-connected applications.

References

[1] Tirthasarathi Lodh, Nataraj Pragallapati, and Vivek Agarwal, "Novel Control Scheme for an Interleaved Flyback Converter based Solar PV Microinverter to Achieve High Efficiency," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3473-3482, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[2] Yong Dae Kwon et al., "Series Resonant Converter-based Full-Bridge DC-DC Partial Power Converter for Solar PV," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 1719-1729, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[3] Poornima Mazumdar, Prasad N. Enjeti, and Robert S. Balog, "Analysis and Design of Smart PV Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 451-459, 2014. [CrossRef] [Google Scholar] [Publisher Link]

[4] Nicholas Falconar, Dawood Shekari Beyragh, and Majid Pahlevani, "An Adaptive Sensorless Control Technique for a Flyback-Type Solar Tile Microinverter," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13554-13562, 2020. [CrossRef] [Google Scholar] [Publisher Link]

[5] Ali Alenezi, and Hussain A. Hussain, "A New Control Approach for Least Processed Power Tracking under Mismatch Conditions in PV Systems using Differential Power Processing," *IEEE Transactions on Industry Applications*, vol. 60, no. 1, pp. 532-543, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[6] Mashood Nasir et al., "Solar PV-based Scalable DC Microgrid for Rural Electrification in Developing Regions," *IEEE Transactions on Sustainable Energy*, vol. 9, no. 1, pp. 390-399, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[7] Hadeed Ahmed Sher et al., "A Single-Stage Stand-alone Photovoltaic Energy System with High Tracking Efficiency," *IEEE Transactions on Sustainable Energy*, vol. 8, no. 2, pp. 755-762, 2017. [CrossRef] [Google Scholar] [Publisher Link]

[8] Amardeep B. Shitole et al., "Soft-Switched High Voltage Gain Boost-Integrated Flyback Converter Interfaced Single-Phase Grid-Tied Inverter for SPV Integration," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 482-493, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[9] Abderezak Lashab et al., "Discrete Model-Predictive-Control-based Maximum Power Point Tracking for PV Systems: Overview and Evaluation," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7273-7287, 2018. [CrossRef] [Google Scholar] [Publisher Link]

[10] Rupali Mohanty et al., "Lower Output Voltage Harmonics with Optimum Switching Angles of Single PV-Source based Reduced Switch Multilevel Inverter using BWO Algorithm," *IEEE Access*, vol. 12, pp. 5054-5065, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[11] Sivanagaraju Gangavarapu, Manish Verma, and Akshay Kumar Rathore, "A Novel Transformerless Single-Stage Grid-Connected Solar Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 970-980, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[12] Arghyadip Bhattacharya, Arup Ratan Paul, and Kishore Chatterjee, "A Coupled Inductor based Ćuk Microinverter for Single Phase Grid Connected PV Applications," *IEEE Transactions on Industry Applications*, vol. 59, no. 1, pp. 981-993, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[13] Saiedeh Khadem Haghighian et al., "A Seventeen-Level Step-up Switched-Capacitor-based Multilevel Inverter with Reduced Charging Current Stress on Capacitors for PV Applications," *IEEE Access*, vol. 11, pp. 118124-118143, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[14] Nabil Karania et al., "Advanced High Switching-Frequency Cascaded H-Bridge Multilevel Inverter based Shunt Active Filter for PV Generation: A Case Study," *IEEE Open Journal of Industry Applications*, vol. 6, pp. 262-280, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[15] Yazeed Yasin Ghadi et al., "An Improved Artificial Neural Network-based Approach for Total Harmonic Distortion Reduction in Cascaded H-Bridge Multilevel Inverters," *IEEE Access*, vol. 11, pp. 127348-127363, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[16] Arkadiusz Lewicki, Charles I. Odeh, and Marcin Morawiec, "Hybridized SVPWM Algorithm for Multilevel CHB Inverter with DC-Link Voltage Control Capability," *IEEE Transactions on Power Electronics*, vol. 39, no. 10, pp. 13248-13261, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[17] Gaël Pongnot et al., "Comparative Analysis of a Low-Voltage CHB Inverter without PWM and Two-Level IGBT/SiC Inverters for Electric Vehicles on Driving Cycles," *IEEE Open Journal of Vehicular Technology*, vol. 6, pp. 542-553, 2025. [CrossRef] [Google Scholar] [Publisher Link]

[18] Supratik Bhowmick et al., "A PSO-based Optimized Hybrid PWM Strategy for a Binary Asymmetric Cascaded H-Bridge Photovoltaic Inverter with Single PV Source Per Phase," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 1654-1665, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[19] Shuvra Prokash Biswas et al., "Advanced Level Shifted Carrier based Bus Clamping PWM Technique for a 54-Pulse AC-DC Converter Fed MLI based Induction Motor Drive," *IEEE Transactions on Industry Applications*, vol. 60, no. 3, pp. 4109-4124, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[20] Mahyar Hassanifar et al., "A Modular Cascaded Multilevel Converter with High Configurability: Design, Analysis, and Optimization Study," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 850-861, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[21] Phani Kumar Chamarthi et al., "Improved PWM Approach for Cascaded Five-Level NPC H-Bridge Configurations in Multilevel Inverter," *IEEE Transactions on Industry Applications*, vol. 60, no. 5, pp. 7048-7060, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[22] Muthukumar Paramasivan et al., "An Alternative Level Enhanced Switching Angle Modulation Schemes for Cascaded H Bridge Multilevel Inverters," *IEEE Access*, vol. 11, pp. 57365-57382, 2023. [CrossRef] [Google Scholar] [Publisher Link]

[23] Thawat Sornsadaeng et al., "A Strategy for Neutral Voltage Modulation Ensuring Fault Tolerance in CHB Multilevel Inverters with Reduced CMV and Unbalanced DC Sources," *IEEE Access*, vol. 12, pp. 154138-154159, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[24] Mehmet Halil Yabalar, and Ergun Ercelebi, "Hybrid Optimization based Harmonic Minimization in Three Phase Multilevel Inverter with Reduced Switch Topology," *IEEE Access*, vol. 12, pp. 71010-71023, 2024. [CrossRef] [Google Scholar] [Publisher Link]

[25] Rohit Kumar, and Bhim Singh, "Development of Fundamental Modulation Technique based Asymmetric Multi-Level Inverter and Multi-Pulse Converter to Prevent Medium Voltage Drive from Harmonic Component," *IEEE Transactions on Industry Applications*, vol. 61, no. 1, pp. 359-369, 2025. [CrossRef] [Google Scholar] [Publisher Link]